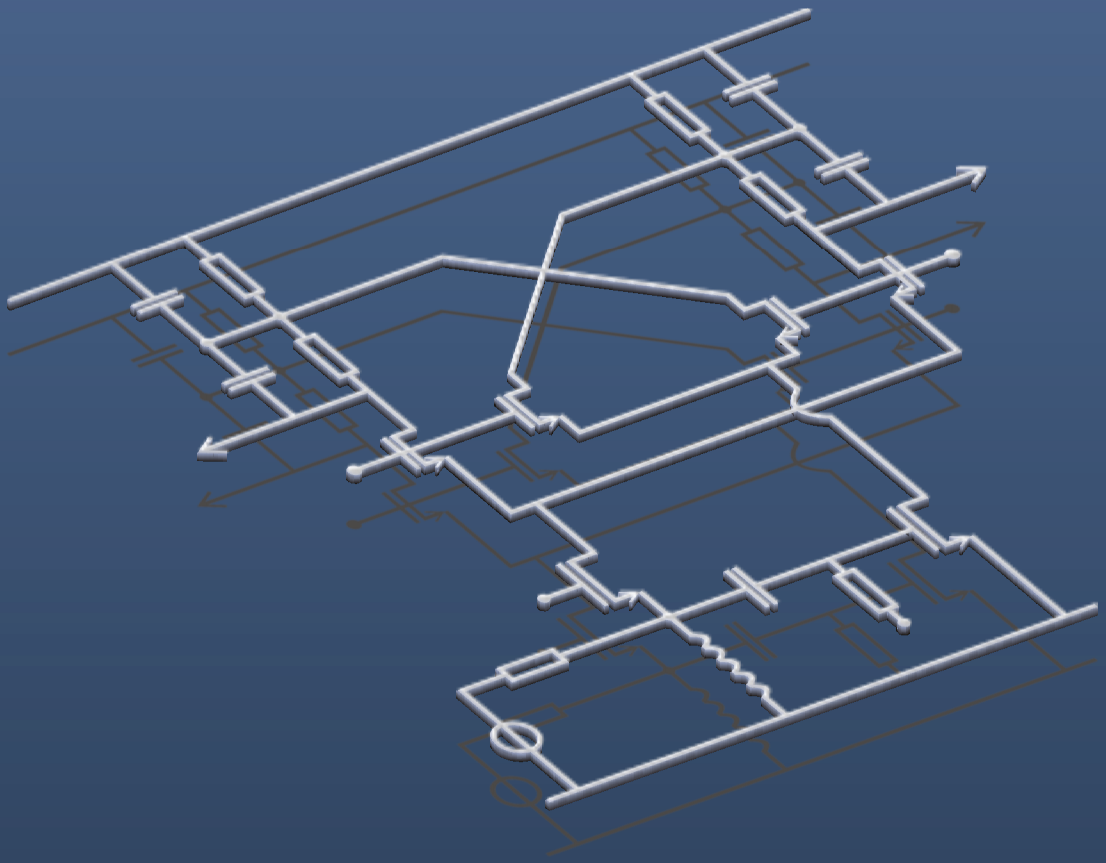
Compact wideband CMOS receiver frontends for wireless communication



Stephan Blaakmeer

COMPACT WIDEBAND CMOS RECEIVER FRONTENDS FOR WIRELESS COMMUNICATION

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COMPACT WIDEBAND CMOS RECEIVER FRONTENDS FOR WIRELESS COMMUNICATION

PROEFSCHRIFT

ter verkrijging van
de graad van doctor aan de Universiteit Twente,
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“Verbeeldingskracht is belangrijker dan kennis.”
– Albert Einstein

Samenvatting

Draadloze communicatie is niet meer weg te denken uit ons dagelijks leven, de mobiele telefoon is hiervan het meest sprekende voorbeeld. Een communicatie verbinding bestaat uit een zender, een ontvanger en het transmissie medium, lucht of vacuüm in het geval van een draadloze verbinding. Een onderdeel van de ontvanger (receiver) is het 'receiver frontend.' Het receiver frontend versterkt het zwakke, hoog frequente signaal dat binnenkomt op de ontvangstantenne en brengt het omlaag in frequentie. Hierna kan met behulp van verdere signaalbewerkingen, inclusief analoog naar digitaal omzetting voor moderne standaarden, de verzonden informatie teruggewonnen worden.

De vraag naar breedband ontvangers neemt toe. Dit wordt veroorzaakt door de opkomst van breedband draadloze standaarden (UWB) en de vraag naar flexibele ontvangers (SDR) die geschikt zijn voor verschillende bestaande en toekomstige communicatie standaarden.

Bestaande ontvangers zijn over het algemeen smalbandig en niet geschikt om breedband signalen te verwerken, voor breedband ontvangers zijn nieuwe receiver frontend topologieën nodig. Om de kosten laag te houden, hebben compacte receiver topologiën gefabriceerd in standaard CMOS processen de voorkeur.

Dit proefschrift richt zich op breedband ontvangers die functioneren tussen enkele honderden megahertz tot rond de tien gigahertz en een bandbreedte van tenminste een paar gigahertz hebben. Voor breedband ontvangers liggen de benodigde versterking, ingangsimpedantie en ruisgetal in dezelfde orde als voor de traditionele smalband ontvangers. De uitdaging bij breedband ontvangers is

om deze specificaties over de gehele bandbreedte te halen. In breedband ontvangers kunnen vele combinaties van stoorzenders tot verstoring in de ontvangstband leiden, dit resulteert in uitdagende eisen aan de lineairiteit.

Aan het begin van dit onderzoek is de ruisonderdrukking (noise canceling) techniek geselecteerd als geschikte kandidaat om breedband ontvangers (receiver frontends) te implementeren. In een voorgaand onderzoek zijn een aantal ruisonderdrukkende circuit topologieën gegenereerd. Een van deze topologieën, de CG-CS topologie, is met name geschikt. Deze topologie combineert twee basis functies van een receiver frontend in een circuit: versterking met lage ruis en de conversie van een ongebalanceerd naar gebalanceerd signaal (balun).

In dit project zijn drie ontwerpen gemaakt. Het CG-autotrafo-CS ontwerp, gebaseerd op de CG-CS topologie, is een breedbandige, ruis arme versterker (LNA) met laag vermogensverbruik en maakt gebruik van een geïntegreerde transformator. Ook het tweede ontwerp, de Balun-LNA, is gebaseerd op de CG-CS topologie. Deze breedband LNA heeft gelijktijdig ruisonderdrukking, distortie-onderdrukking en een goed gebalanceerd uitgangssignaal. De BLIXER topologie is een verdere ontwikkeling van de CG-CS topologie. Naast balun en LNA-functionaliteit brengt dit breedbandige circuit het signaal omlaag in frequentie.

Tijdens dit project is de interesse in breedband LNA's en receiver frontends aanzienlijk toegenomen. Slechts twee circuit technieken uit de literatuur zijn geschikt voor de implementatie van *compacte* breedband LNA's: negatieve terugkoppeling en ruisonderdrukking. Van de twee LNA's beschreven in dit proefschrift komt vooral de Balun-LNA goed uit de vergelijking met andere ontwerpen uit de literatuur. De sterke punten van de BLIXER in vergelijking met andere breedband receiver frontends zijn oppervlakte en RF-bandbreedte, ook de overige eigenschappen zijn concurrerend. De BLIXER topologie is zeer geschikt voor de realisatie van compacte breedband receiver frontends voor draadloze communicatie.

Abstract

Wireless communication is an integral part of our daily life, the mobile phone is an example of a very popular wireless communication device. A communication link consists of a transmitter, a receiver and the transmission medium, which air or vacuum for a wireless link. Part of the receiver is the receiver frontend. The receiver frontend amplifies the weak, high frequency, signal received at the receiver antenna and brings the signal down in frequency. Using further signal processing, including analog-to-digital conversion for modern standards, the message sent by the transmitter can be recovered.

There is an increasing demand for wideband receiver frontends. This is due to the emerge of wideband wireless standards (UWB) and due to the desire for flexible radios (SDR), which can comply to multiple existing and future communication standards.

Existing receiver topologies are generally narrowband and not suited for wideband operation, consequently there is a need for new wideband receiver topologies. For low cost solutions, compact receiver topologies implemented in mainstream CMOS technology are preferred.

In this thesis, wideband receiver operation between a few hundreds of megahertz up to around ten gigahertz, with an input bandwidth of at least a few gigahertz is aimed at. For wideband receivers the required gain, input impedance and noise figure are in the same order as for traditional narrowband receivers. The challenge in wideband receivers is to meet all these specifications across its entire bandwidth. Due to the wideband nature there are many

interferer combinations that lead to in-band distortion in wideband receivers, resulting in challenging linearity requirements.

At the start of this research project, the noise canceling technique was identified as a suitable candidate to implement wideband receiver frontends. In a preceding research project a number of noise canceling topologies were generated. One of these topologies, the CG-CS topology, is especially useful as it implements two basic receiver frontend functions, low noise amplification and single-ended to differential conversion (balun), into one circuit core.

Three designs are implemented during this research project. The CG-autotrafo-CS design, based on the CG-CS topology, yields a low-power, wideband, low-noise amplifier (LNA) and uses an on-chip transformer. The second designs, the Balun-LNA is also based on the CG-CS topology. This is a wideband LNA design that simultaneously achieves noise canceling, distortion canceling and a well-balanced output signal. The BLIXER topology is a further evolution of the CG-CS topology. Next to balun and LNA-functionality complex frequency down-conversion is realized, all in a single wideband circuit core.

During the course of this project, the interest in circuits in wideband LNAs and receiver frontends has increased significantly. Only two circuit techniques found in literature are suitable to implement *compact* wideband LNAs: negative feedback and noise canceling. From the two LNAs described in this thesis especially the Balun-LNA compares favorably to other designs found in literature. The BLIXER stands out on area and RF-bandwidth when compared with other wideband receiver frontends, while other characteristics are competitive. The BLIXER topology is very suitable for the implementation of compact wideband receiver frontends for wireless communication.

Contents

Chapter 1

Introduction

1.1 Wireless communication

Wireless communication is becoming more and more popular. One of the most commonly used wireless communication devices is the mobile phone. There are many more examples of wireless communication such as WLAN (or WiFi), Bluetooth, Global Positioning System (GPS) and Digital Video Broadcasting (DVB). Next to the increased usage of wireless communication there is an increasing demand for broadband communication. Figure 1.1 shows that the number of mobile broadband subscriptions has increased rapidly over the recent years.

Using wireless communication, information is carried from the transmitter to the receiver through the air[1]. The transmitter conditions the information signal such that it can be transmitted using radio waves. At the receiver-side, the antenna picks-up the radio waves. The receiver converts this signal to an amplitude level and frequency range that is suitable for further (often digital) signal processing. After signal processing, the information sent by the transmitter is recovered at the receiver side.

[1] For an earth-based communication system.

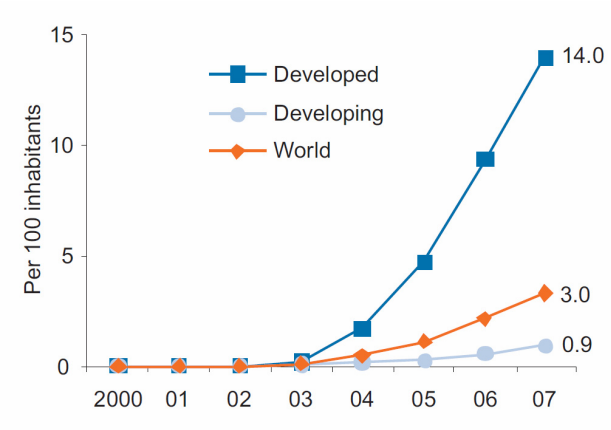

Figure 1.1: Number of mobile broadband[1] subscriptions per 100 inhabitants [1].

Wires and cables are commonly used for communication connections. However, consumers prefer to use equipment in a mobile, hence wireless, way. The increased use of laptops, netbooks, PDAs and MP3-players leads to a strong increase in wireless data communication. To support this increase, more bandwidth is needed and innovations to support larger bandwidths are desired.

In the next section the receiver will be discussed in more detail.

1.2 Receiver frontend

Figure 1.2 shows the block diagram of a typical receiver for wireless communication. The major part of the receiver is nowadays implemented as an integrated circuit (IC), or chip. The antenna and a band filter are usually placed off-chip. The antenna converts the

[1] In this case *broadband* refers to the bandwidth, in bits per second, of a data connection. Next to this usage, *broadband* is often used as synonym for *wideband*. The term *wideband* refers to systems that operate across a high bandwidth of the radio spectrum. The terms *wideband* and *broadband* are closely related as *wideband systems* enable *broadband data connections*.

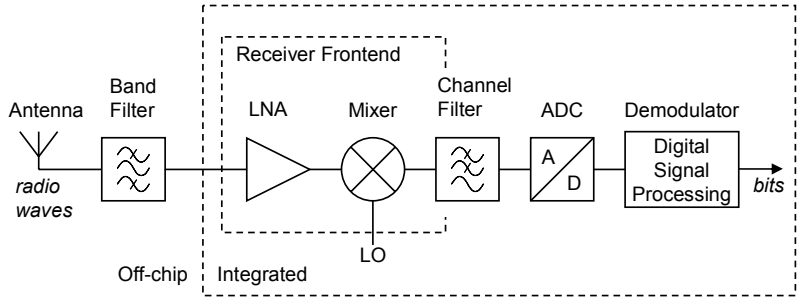

Figure 1.2: Block diagram of a receiver for wireless digital communication.

electromagnetic wave to a radio frequency (RF) electrical signal. The band filter selects the radio band of interest and removes potentially strong out-of-band signals (sometimes also referred to as RF pre-select filter). The integrated part of the receiver usually starts with a Low Noise Amplifier (LNA). It presents suitable impedance to the antenna or pre-select filter and amplifies the weak antenna signals. The LNA is generally followed by a down-conversion mixer. By multiplying the output signal of the LNA with the local oscillator (LO) signal, the high-frequency radio signal is converted down to a lower frequency, often the baseband ("zero-IF receiver"). The signal can then be filtered by a low-pass filter to select the relevant band and perform anti-alias filtering before A/D-conversion. The A/D-converter (ADC) converts the analog output signal of the channel filter into a digital signal (bits). From this digital stream of bits the information send out by transmitter can be recovered using digital signal processing.

This thesis deals with the first part of the receiver, referred to as the "receiver frontend," as it is the first part of the integrated circuit that interfaces to the external world. As indicated in Figure 1.2, the receiver frontend consists of the LNA and the mixer. The first section of the channel-filter is often also taken into account as it can be realized in the output stage of the mixer. Overall, the function of the receiver frontend is to amplify the often weak signal at the output of the band-filter and bring it down to a frequency range that is suitable

for the ADC. Compared to direct A/D-conversion of the RF signal, this strongly relaxes ADC requirements and baseband filter requirements, as the typical bandwidth of an RF signal is only a small fraction of the RF center-frequency. Furthermore, low-pass filtering in front of the ADC helps to bring down the dynamic range and to reduce the required number of bits in the ADC. Note that the amplification and frequency conversion of the signal should be done without adding much noise or distortion, to avoid degradation of the receiver sensitivity.

1.3 Trends in wideband receiver frontends

As discussed in section 1.1, there is an increasing demand for wireless communication with higher data-rates. The quest for higher data-rates lead to the initiation and the development of new wideband communication standards, for instance WiMedia UWB. This will be discussed in more detail in section 1.3.1.

Another trend is the ever increasing wireless functionality that is expected from mobile devices like phones, PDAs, laptops, netbooks, etc. A typical high-end phone (or smart phone) nowadays supports GSM, UMTS (3G), WLAN (also known as WiFi or IEEE 801.11b and IEEE 801,11g), Bluetooth, GPS and FM-radio. Some phones already incorporate mobile digital television (DVB-H) [2] and new standards for instance WiMedia UWB [3], and (pre) 4G-standards like WiMAX [4] and LTE [5] are under consideration. Integrating more and more of these standards into one mobile device, while keeping the costs low and the devices small, also asks for wideband receiver frontends. This is discussed in more detail in section 1.3.2.

1.3.1 Ultra-wideband communication

In February 2002 the Federal Communications Committee (FCC) opened up a large part of the radio spectrum for the so called ultra-wideband (UWB) technology [6]. One of the motivations to allow UWB technology is to make short-range (up to about 10 meter), high-speed data transmissions (a few hundred of Mbps) possible. Both in-house and office applications are anticipated, e.g. fast exchange of data between a mobile device (MP3 player, PDA, phone, etc.) and a PC.

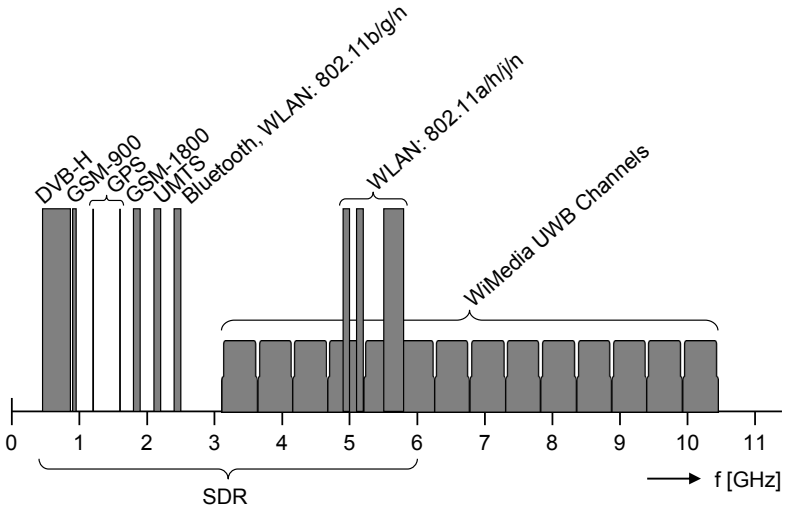

Figure 1.3: Operation frequencies of wireless standards.

One of the foreseen killer applications of UWB is Wireless USB. Wireless USB is the cable-less variant of USB2.0 (up to 480 Mbps), the de facto PC peripheral standard. Other emerging high-speed data links may include wireless streaming of HD video signals, removing the cables between DVD-players or laptops and TVs.

Figure 1.3 shows the channel frequency specification of the UWB standard proposed by the WiMedia alliance [7]. The frequency range assigned to UWB communication systems (3.1–10.6 GHz) is one to two orders of magnitude wider than the frequency band assigned to traditional narrow-band communication standards, which are also shown in Figure 1.3. This large bandwidth strongly affects the frontend of the receiver.

Traditional radio receiver frontends are designed for a small fractional bandwidth. Therefore, in order to implement UWB transceivers, new wideband receiver frontend topologies are required.

1.3.2 Software defined radio

As discussed before, more and more wireless functionality is integrated in portable devices like smart phones. Smart phones are relatively bulky and costly compared to the more common, plain mobile phones. Next to their GSM functionality, these phones are capable of supporting several other wireless standards. Without changes in architecture these phones have a dedicated receiver frontend, including bulky off-chip filters and antennas, for every standard. For costs and size reasons, it is 'smarter' to use one receiver that can handle all standards.

A Software Defined Radio (SDR) [8] is a radio that is configurable using software. The software, running on a hardware core, can be programmed to demodulate signals from (ideally) any, also future, standards. The software defines the radio functionality, hence the name Software Defined Radio. Figure 1.3 shows where commonly used wireless standards are located in the spectrum. A receiver that is able to receive all these different standards has to be either narrowband and tunable over a large bandwidth, or have a bandwidth that is large enough to cover most standards.

A narrowband, tunable, frontend requires inductors, which conflicts with the demand for compactness as discussed in the next section. Next to this, the center frequency of a narrowband circuit (f_C) is proportional to the square root of the product of the used capacitor (C) and inductor (L) values ($f_C \sim 1/\sqrt{LC}$). For tuning across a large bandwidth a high ratio of maximal over minimal capacitance (or inductance) is required, which complicates the implementation in practice.

As the practical implementation of narrowband receivers with a large tuning range is troublesome, new wideband receiver frontend topologies that are required for the implementation multi-standard, multi-band Software Defined Radios.

1.4 Compact CMOS

Modern wireless communication standards as the ones mentioned in section 1.3 all rely heavily on digital processing [9]. Complex algorithms like FFTs, iFFTs, etc. are performed in the (de)modulation process. The mainstream IC technology for digital signal processing is CMOS. The natural choice to obtain low-cost transceivers [1] is integrating the (RF & analog) receiver and transmitter frontend together with the digital signal processing backend into a System on a Chip (SoC). For chips aimed at consumer applications it is of key importance to keep their costs as low as possible. As the price of a chip is proportional to its area, the frontend should occupy a as little as possible chip area. Therefore 'compact' frontend designs are required for low-cost transceivers.

Inductors are often used in RF circuit design. However, an integrated inductor occupies large chip area, which conflicts with the desire for compact designs. Therefore, frontend designs which require no integrated inductors are preferred.

Another aspect of compactness is the amount of external components that is needed. If external components can be avoided this tends to reduce the costs of the transceiver system significantly. This holds for the band filters, but also for auxiliary components like baluns, which are used to interface a single-ended antenna to the differential signals often used on-chip. Finally, combined antennas covering multiple bands, in combination with a combined RF pre-select filter also help to reduce overall size. In conclusion, methods and techniques to reduce the number of external components and to minimize chip area are desired to reduce receiver cost and size.

1.5 Motivation and aim

In November 2003 a project on "Ultra-wideband techniques in CMOS" was started in the IC-Design group of the University of Twente in cooperation with Philips Research Eindhoven, which later on became

[1] A transceiver is the combination of a transmitter and receiver.

NXP Research Laboratories. This project was triggered by both the quest for wideband receivers, especially for UWB, and the innovations from the IC-Design group on "Noise Canceling" [10-11].

At the start of the project, Philips already had started the development of UWB products. The high-frequency frontend was under development in dedicated high-frequency IC technologies like SiGe-bipolar, while the digital backend would be implemented in CMOS. For future generations of UWB products highly integrated complete CMOS solutions were anticipated. The noise canceling technique was seen as a potential interesting technique as it renders low noise over a wide band. Moreover, using the same technique, also distortion canceling seemed to be possible. In the thesis of F. Bruccoleri [11] a number of noise canceling circuit alternatives were proposed. Several of these circuit alternatives were still unexplored and asked for more research.

A PhD project was hence defined with the aim to ***explore the noise canceling technique*** for wideband applications and ***develop wideband receiver circuit topologies in CMOS***.

More concretely, based on UWB specifications [12] and previous SDR research [13], a receiver frontend with roughly the following properties is aimed at:

- A wide receiver band, preferably covering the complete UWB range (3–10 GHz) and the SDR range (0.4–6 GHz).
- An input impedance of 50 Ω to match to an antenna or band filter.
- Sufficient gain to mitigate the noise of stages within the frontend (mixer) and stages following the frontend, (baseband filters, amplifiers and ADC)
- A noise figure below 5 dB for the integrated part of the receiver.
- Sufficient linearity to handle both second and third order intermodulation products in different interferer scenarios. High linearity relaxes the band filter selectivity requirements.
- A compact, highly integrated, CMOS circuit to minimize cost and size.

- A power budget in the order of tens of milliwatts, so that the power dissipation is not dominated by the receiver frontend but by the ADC and digital signal processing.

These properties and their background will be discussed in more detail in Chapter 2.

1.6 Thesis outline

This thesis will explore wideband receiver techniques with focus on noise canceling circuit topologies and is constructed as follows. Chapter 2 discusses requirements and circuit topologies for wideband receiver frontends. The specifications mentioned in the previous section are discussed, focusing on similarities and differences of wideband receivers compared to traditional narrowband receivers. These differences lead to additional challenges in the design of wideband receivers which will be identified. Furthermore, an overview of circuit topologies known from literature, at the start the project is given. As part of that, the known noise canceling topologies are discussed. A particular topology which exploits parallel common-gate and common-source stages (the CG-CS topology) is selected as an attractive candidate topology for further research.

In Chapter 3 the CG-CS topology is explored, where a compact wideband transformer is used to realize voltage gain at low power. An LNA for the 3–5 GHz UWB sub-band is realized on chip and measurements are reported [14].

In Chapter 4 the CG-CS topology without using a transformer is explored further and compared to previous CG-CS LNA implementations. It turns out that it is possible to dimension the circuit such that it simultaneously realizes a balanced output, and achieves noise canceling and distortion canceling of the noise and distortion of the common-gate transistor. This is exploited to realize a Balun-LNA with high 2nd order non-linearity, exploiting an optimum distortion point in the common-source stage [15-16].

In Chapter 5 a wideband receiver topology is introduced that combines balun, LNA and the mixer functionality in a single circuit.

This topology uses V-I conversion at RF immediately followed by current-switching for down-conversion. This allows for realizing a large RF-bandwidth. It also renders a linearity advantage as only one non-linear (V-to-I) conversion contributes distortion at high frequencies. The circuit is referred to as the BLIXER, as it stacks a Balun-LNA and a mixer. In the topology the LNA current is re-used in the mixers, which is beneficial for the overall power consumption [17-18].

In Chapter 6 the relation between the designs of Chapter 3–5 and their performance is reviewed. Moreover, the designs are put into perspective by comparing them to results attained by other groups during the course of this project.

Finally Chapter 7 summarizes the contents of the thesis, and its main conclusions. Furthermore, its original contributions are identified and recommendations for further work are given.

Chapter 2

Wideband receiver frontends – Requirements and circuit techniques

2.1 Introduction

The block diagram of a receiver shown in Figure 1.2 is valid for both narrowband and wideband receivers. Narrowband and wideband receivers use the same circuit blocks; in both LNAs, mixers, filters, etc. are used. However, in wideband receivers the requirements on these blocks are more challenging compared to narrowband receivers, as will be discussed in section 2.2. Furthermore, this chapter describes circuit techniques for wideband receivers as known at the start of the project. The main question is whether these techniques are suitable for the implementation of compact wideband CMOS receivers. The techniques will serve later on in the thesis as comparison material. From the available techniques the noise canceling technique is recognized as a promising technique. The noise canceling CS-CG topology is identified as very suitable for compact receivers as it integrates a balun and LNA and shows good performance to competing noise canceling topologies [11]. This topology will be the basis for the circuits in Chapter 3 to 5.

2.2 Requirements for wideband receivers

The various requirements for wideband receivers will be discussed one by one in the following sections, focusing on how they are different from the narrowband case.

2.2.1 Bandwidth

Ultra-wideband (UWB) is defined by the FCC as radio systems that have a bandwidth exceeding the lesser of 500 MHz or 20% of its center frequency [19]. In this thesis we follow this definition to classify a receiver as wideband. Commonly used wireless communication standards (GSM, WLAN, Bluetooth, etc.) have channel-bandwidths of 0.2–20 MHz and use an RF-band of typically several tens of MHz. In UWB systems the bandwidth must be at least 500 MHz, which is more than an order of magnitude larger than in traditional systems.

In this thesis, receivers with a bandwidth in the order of a few GHz are aimed for. To cover all UWB sub-bands at once, a bandwidth of 7.5 GHz is required (3.1 – 10.6 GHz). For SDR systems, a useful bandwidth of about 6 GHz is often aimed at [20]. This is because most commonly used wireless communication standards operate in the frequency range of a few hundreds of megahertz up to roughly 6 GHz, as was shown in Figure 1.3.

The challenge in wideband receiver design is to achieve the required performance on gain, input impedance, noise figure and linearity etc. across the entire RF-bandwidth.

2.2.2 Gain and noise

In a receiver frontend RF-gain, the gain at the radio frequencies, is provided by the low noise amplifier (LNA). RF-gain is required to suppress the contribution of the noise produced in the mixer and subsequent stages to the overall noise. The required gain of the LNA in order to obtain a certain receiver noise figure ($NF_{Receiver}$)[1] can be calculated using the well-known equation of Friis [21]:

[1] The noise figure (NF) is the noise factor (F) expressed in decibels (dB).

$$F_{Receiver} = F_{LNA} + \frac{F_{Mix} - 1}{G_{A,LNA}} \quad \Leftrightarrow \tag{2–1}$$

$$G_{A,LNA} = \frac{F_{Mix} - 1}{F_{Receiver} - F_{LNA}} \tag{2–2}$$

where F_{LNA} is the noise figure of the LNA, $G_{A,\,LNA}$ is the available gain of the LNA and F_{Mix} is the aggregate noise figure of the mixer and circuits following the mixer.

Assuming a noise figure of 6 dB is acceptable for an UWB receiver and we assume a preceding passive reciprocal band filter to have 1 dB loss and hence 1 dB noise figure, then the required noise figure becomes: $NF_{Receiver}$ = 5 dB. Assuming NF_{LNA} = 4 dB, and NF_{Mix} = 12 dB. Using equation (2–2) it follows that the required available power gain of the LNA is: $G_{A,\,LNA}$ = 14 dB.

Active mixer topologies often have a gate of a transistor as input. Therefore, instead of the input power, the input voltage of the mixer is of importance. The voltage gain (A_V) is then a more appropriate measure of gain than available gain (G_A). The voltage gain of a circuit is determined without loading it, whereas available gain is determined using a matched load. The matched load halves the voltage swing at the output and the voltage gain is 2 times (6 dB) larger than the available power gain. The required voltage gain in the example above equals: $A_{V,LNA} = G_{A,LNA}$ + 6 dB = 20 dB.

The above calculated RF-gain is in the same order as the required gain in narrowband receivers. The required noise figure of narrowband receives may be lower than the above assumed 5 dB. Lower receiver noise figures are generally obtained by an LNA with lower noise figure. This keeps the denominator of (2–2) roughly equal, as both $F_{Receiver}$ and F_{LNA} decrease. Most mixer topologies used in narrowband receivers are suitable for wideband operation and their noise is flat over a large bandwidth, thus also the numerator of (2–2) is equal for narrow- and wideband receivers. Consequently, the required RF-gain for narrow- and wideband receivers is in the same

order. The challenge in wideband receivers is to maintain the gain over a large bandwidth.

2.2.3 Input impedance

Radio communication systems are generally designed using a characteristic impedance (Z_0) of 50 Ω. This means that antennas, filters and transmission lines operate optimal when terminated with a 50 Ω impedance. In case of an impedance mismatch at the input of the chip, part of the incoming signal power will be reflected. The return loss (RL) is defined as the ratio of the reflected (P_r) and incoming, or incident, signal power (P_i). Next to the ratio of reflected and incoming power, the return loss can be expressed in terms of input impedance (Z_{in}) and characteristic impedance (Z_0):

$$RL = 10 \cdot log\left(\frac{P_r}{P_i}\right) = 20 \cdot log\frac{|Z_{in} - Z_0|}{|Z_{in} + Z_0|} = S_{11} \quad [dB] \qquad (2\text{–}3)$$

Where S_{11} is the input voltage reflection coefficient, which is equivalent to the return loss. S_{11} is generally used to denote the quality of the input impedance match.

The optimal situation occurs when input impedance (Z_{in}) equals the characteristic impedance (Z_0), thus when $S_{11} \rightarrow -\infty$ dB. In that case the amount of reflected power is zero and all signal power is available on the chip. For many commercial radio systems the input impedance is considered to be acceptable when $S_{11} < -10$ dB, i.e. when less than 10% of the incoming signal power is reflected at the input of the chip.

Both for narrowband and wideband receivers a certain frequency range is required in which S_{11} is lower than –10 dB. The difference is that for a wideband receiver this frequency range needs to be much wider, which makes the design more challenging.

2.2.4 Noise figure

The sensitivity of a receiver is defined as the minimum signal level ($P_{in,min}$) that the system can detect with acceptable signal-to-noise ratio [9]:

$$P_{in,\min|dBm} = P_{RS|dBm/Hz} + NF_{|dB} + SNR_{\min|dB} + 10 \cdot \log B \qquad (2\text{–}4)$$

where P_{RS} is the available noise power of the signal source (kT = –174 dBm/Hz at T = 300 K). SNR_{min} denotes the minimal signal-to-noise ratio that is required to demodulate the received signal with a given bit error rate (BER). B is the channel bandwidth of the received signal in hertz. And finally, NF is the noise figure of the receiver. Decreasing the noise figure, improves the sensitivity of a receiver. A better sensitivity means that, for a given transmit power, a larger distance can be bridged between transmitter and receiver. Therefore, the noise figure is an important parameter of a receiver.

The challenge for wideband receivers is that the RF-bandwidth where low noise needs to be a achieved is much larger than in narrowband receivers. Traditional narrowband techniques often obtain low noise exploiting resonating high-Q LC-tanks [22]. However, wideband circuit techniques that achieve low noise without resorting to the use of inductors are desired. In this thesis, we aim for a receivers with a noise figure in the order of 4–5 dB.

2.2.5 Linearity

The reception of a wanted signal can be hampered when unwanted signals, or interferers, are present in the radio spectrum. Due to non-linearity in the receiver, interferer combinations can produce intermodulation products that distort the wanted signal. Intermodulation products arising from second order (quadratic) and from third order non-linearity are generally dominant.

In radio systems the amount of non-linearity is often quantified using the input referred intercept point. For second order non-linearity, the second order input referred intercept point (IIP2) is used, and for third order non-linearity (IIP3) is used.

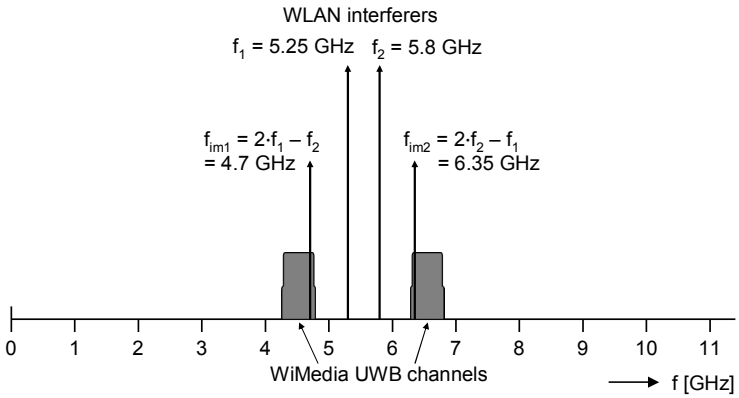

Figure 2.1: Third order intermodulation distortion in a WiMedia UWB receiver.

Third order intermodulation distortion

For most narrowband standards an IIP3 of around -10 dBm is enough to handle in-band interferers [23]. Out-of-band interferers are suppressed by the band-filter to levels that can be handled by the narrowband receiver.

In [24] the required linearity of a wideband WiMedia UWB receiver (at that time still called MBOA-UWB) for different interferer scenarios is derived. To calculate the required IIP3 an interferer scenario of two 802.11a (WLAN) interferers is used, which is shown in Figure 2.1. The required IIP3 for the wideband receiver is -9 dBm, where 20 dB pre-filtering of the interferers is assumed. In absence of pre-filtering, the IIP3 requirement becomes as high as +21 dBm.

A wideband receiver with high linearity requires less pre-filtering to withstand interferes. Less or no pre-filtering makes the total receiver more flexible and low-cost. In this thesis we aim at wideband receivers with an IIP3 in the order of 0 dBm.

Second order intermodulation distortion

In a receiver the RF-signal is down-converted to the IF-band by the mixer. In the mixer there are three mechanisms that lead to second order intermodulation distortion [25]:

- Self mixing caused by leakage of the wanted signal from the RF-port to the LO-port of the mixer, which produces an intermodulation product at the IF-output (even in case of a perfect multiplier).
- Second order non-linearity of the LNA and mixer RF-input producing a low-frequency intermodulation product. This product leaks through the mixer from RF-input to IF-output and falls on the wanted signal at IF-output of the mixer.
- Second order non-linearity of the switching core of the mixer producing an intermodulation product at the IF-output of the mixer.

The effects of self mixing can be minimized using careful layout to minimize coupling between the RF and the LO-port and by maximizing the amplitude of the LO-signal. The effects of LNA and mixer-input non-linearity can be minimized using a fully differential, double-balanced mixer topology. Furthermore, the low frequency intermodulation product can be filtered out using AC-coupling between the mixer input stage and the switching core of the mixer. In contrast to the first two mechanisms, the switching core non-linearity is intrinsic to the mixer operation. This mechanism determines the maximal achievable IIP2 of the mixer. Still, by careful design, mixers with IIP2 figures in excess of +65 dBm in 0.18 µm CMOS are possible and even higher IIP2s can be expected in more scaled technologies [25].

The mechanisms described above are present in both narrowband and wideband receivers. They have in common that the wanted signal is distorted at the mixer IF-output, thus *after* the frequency translation from RF to IF has taken place. In this thesis the term 'RF-to-IF IIP2' is used to characterize this type of second order linearity.

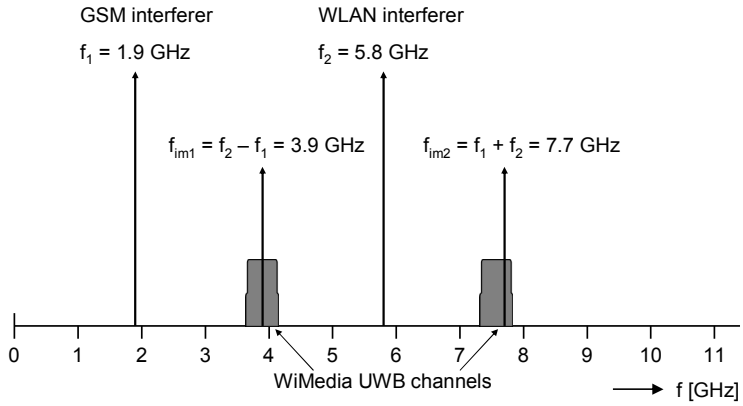

Figure 2.2: Second order intermodulation distortion in a WiMedia UWB receiver.

In a wideband receiver, there is yet another source of second order intermodulation distortion. Non-linearity of the LNA and mixer input stage combined with interferers can lead to second order intermodulation products that fall within the RF-band. This means that the wanted signal is already distorted by interferers *before* the frequency translation. In contrast to the mechanisms described before, higher linearity can not be obtained by reducing mixer leakage or applying AC-coupling. Therefore, the non-linearity of the LNA and mixer-input (RF non-linearity) is the dominant source of second order intermodulation distortion ('RF-to-RF IIP2') in a wideband receiver.

As an example assume a WiMedia UWB (or: MBOA-UWB in [24]) receiver subject to an IEEE802.11a (WLAN) interferer and a PCS/GSM1900 interferer. Second order non-linearity produces two intermodulation terms (at 3.9 and 7.7 GHz) that fall within the UWB frequency band (3.1 – 10.6 GHz), as shown in Figure 2.2. Assuming 20 dB pre-filtering, realistic distances (0.2m and 1m) and maximal transmit power of both interferers, the required IIP2 of the UWB receiver is above +20 dBm [24].

In this thesis the aim is to obtain frontends with enough RF-linearity to achieve an RF-to-RF IIP2 of at least +20 dBm.

2.2.6 Power consumption

Wideband receivers designed for wireless communication will be used in portable products; i.e. battery powered products. To maximize battery live or 'talk-time' the power consumption of the system should be minimized. The increased bandwidth of a wideband receiver should not come at the expense of a dramatic increase of power consumption compared to narrowband receivers. The aim is to keep the power consumption of the wideband receiver frontends in the order of some tens of milliwatts.

2.2.7 Compactness

Transceivers targeted for consumer electronics need to be low cost systems. The costs of a system has a strong relation with its compactness. The compactness is characterized by two aspects; the number of required components, i.e. the number chips and external components in the system, and the required chip-area.

Minimizing the number of external components, such as capacitors, inductors, filters and baluns, and using a single chip solution yields a compact system. In a single chip, the analog high-frequency transceiver frontend is combined with the digital signal processing backend. The digital processing part determines the process choice; a high-density CMOS process. In order to minimize the costs, the total active area needs to be minimized. This asks for a compact design of the analog high-frequency transceiver frontend.

The most area consuming components used in high frequency design are integrated inductors. The area occupied by an integrated inductor can be equivalent a complete digital signal processing core. Therefore, for compact, low cost, transceiver design it is important to minimize the number of integrated inductors.

2.3 Wideband circuit techniques

The first stage of a wideband receiver is the low noise amplifier (LNA). The LNA provides wideband signal amplification (RF-gain) and has a real input impedance, in most cases 50 Ω. Other specifications, which preferably are minimized, are the noise, non-linearity and power consumption.

At the start of this project (early 2004) there were a few different circuit techniques for wideband amplification available. These circuits are reviewed in the following sections and their suitability for compact wideband receiver frontends is discussed.

2.3.1 Distributed amplifier

The distributed amplifier (DA) principle was patented by Percival in 1937 [26]. In the DA-principle a number of amplifying stages is connected using transmission lines, and a traveling wave is amplified along the chain of amplifier stages. The biggest merit of the DA-principle is that the gain-bandwidth product increases with the number of stages. Figure 2.3 shows a typical example of an integrated distributed amplifier [27], where LC-sections are used as artificial transmission lines. A differential DA is published in [28].

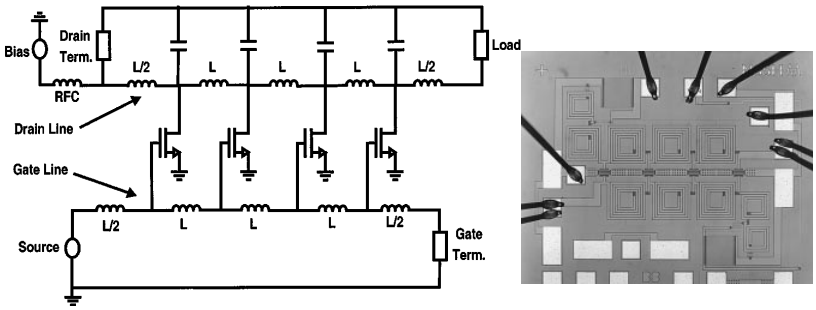

Figure 2.3: Integrated distributed [27], schematic (left) and chip photo (right). The inductors dominate the chip area (0.79 mm^2).

From Figure 2.3 it is clear that the DA-technique is not suitable for the integration of a *compact* wideband receiver as many integrated inductors are required. Next to this, the power consumption of DAs is generally high as it consists of a parallel number of RF-amplifiers in parallel.

2.3.2 Input-filter technique

Two years after the news release of the FCC on UWB [6] the first two LNAs specifically targeted for UWB were presented at the 2004 IEEE International Solid State Circuits Conference (ISSCC) [29-30]. Both topologies were based on a well known (narrowband) LNA principle, inductive degeneration of a common-source stage [22]. The bandwidth of the input match (S_{11}) is extended by adsorbing the input impedance of the inductive degenerated input stage into a multiple section, wideband, band-pass filter.

The wideband CMOS LNA of [29], shown in Figure 2.4, indeed obtains a wideband input match (2.6 – 11.5 GHz). However, the losses associated with the input filter result in a modest noise figure (NF < 6 dB for 2.5 – 8 GHz). A reasonable power gain (10 dB) is obtained and the power consumption is low (9 mW). The required circuit area is large, see inset of Figure 2.4, as five integrated inductors are used.

In [30] a wideband LNA is presented which achieves higher gain and similar matching bandwidth compared to the circuit in [29]. The noise figure is lower as a parallel LC-tank is used at the input. Next to this, bipolar transistors are used, which show lower noise and higher gain (transconductance) than CMOS transistors for a given current. However, this circuit consumes three times more power than [29] and it is implemented a SiGe BiCMOS process, which is a more expensive solution than pure CMOS. Still, four integrated inductors are used and a large circuit area is required.

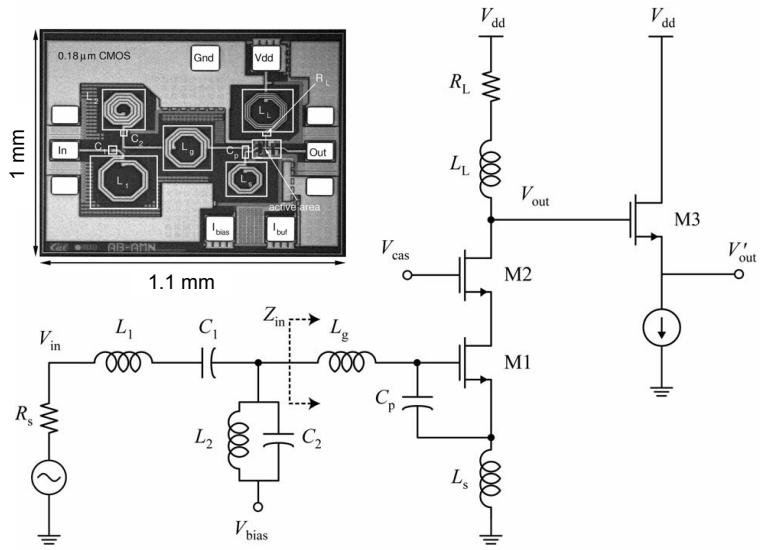

Figure 2.4: Wideband LNA based on an input-filter topology [29], circuit and chip photo (top left).

In conclusion, an LNA based on the input-filter technique requires too many inductors for the implementation of a compact wideband receiver.

2.3.3 Negative feedback technique

The negative feedback technique is well known amplifier principle that was invented by H.S. Black in 1927 and patented in 1937 [31]. High linearity and good noise performance can be obtained in a negative feedback amplifier when the closed loop gain is low compared to the open loop gain of the amplifier. Essentially the difference between open- and closed-loop gain can be used to improve the linearity or noise performance. Next to this, the transfer function of the amplifier and in- and output impedances of an amplifier can be accurately fixed. In contrast to the techniques described in section 2.3.1 and 2.3.2, the negative feedback principle does not rely on the use of inductors. Therefore, it is potentially a circuit technique for the implementation of *compact* wideband receiver frontends. However,

there are two challenges in wideband negative feedback amplifier design. First of all, it is hard to obtain enough loop gain at high frequencies. Furthermore, ensuring stability under all conditions is a challenge.

At the start of this project, the field of wideband CMOS LNAs based on negative feedback was still quite unexplored. Up to 2004 only a few publications dated on this topic can be found in literature.

In [32] a negative feedback amplifier is presented, which has high gain (25 dB) and low noise figure (~3 dB). The amplifier has four internal poles, for stability reasons an on-chip inductor is used and it operates on a limited bandwidth (0.4 – 1.2 GHz). Furthermore, the power consumption of this amplifier is high (35mW).

In [33] and [34], inductorless LNAs based on resistive negative feedback were published, which are in principle wideband. These differential circuits are driven by an external, narrowband, balun and were characterized at only a single frequency (2.1 and 2.4 GHz, respectively). Clearly, the focus was not on wideband amplifiers and receivers at the time (2002).

Around 2003 the interest in wideband receivers increased. This is apparent from the fact that three publications on wideband (low noise) amplifiers were published [35-37] at a single conference (ESSCIRC 2003). The performance of the inductorless negative feedback amplifier of [35] is measured around 900 MHz, 1.8 GHz and 2.4GHz. Around 2.4 GHz it achieves high gain (18 dB) and moderate noise figure (4.6 dB), while consuming 36mW.

The negative feedback amplifiers published up to 2004 clearly had not enough bandwidth to operate in the UWB frequencies (3.1 – 10.6 GHz) or SDR range (– 6 GHz). Furthermore, implemented in CMOS processes with a relative low f_T and pushing for large bandwidth, the power consumption of those circuits was relatively high. On the other hand, f_T increases with every new CMOS generation, which allows the implementation of negative feedback amplifiers with larger bandwidths and lower power consumption. As negative feedback is a well-known technique, much research activity was to be

expected in the quest for wideband receiver frontends. However, we opted to use the less well-known, but promising, noise canceling technique, which is discussed in the next section.

2.3.4 Noise canceling technique

The noise canceling technique was invented in the IC-Design group of the University of Twente [10, 38-39]. The wideband LNA published in [39] and [40], which exploits the noise canceling technique, has interesting properties. Although the power consumption is on the high side (36 mW), it achieves a low noise figure (<2.4 dB) over a large bandwidth (0.15 – 2 GHz). In fact, this work was the starting point and one of the main motivations of this research on "Compact wideband CMOS receiver frontends for wireless communication."

Similar to negative feedback, the noise canceling technique breaks the relation of input impedance of an amplifier and its noise figure. Using the noise canceling technique, the noise of the transistor that determines the input impedance, which is normally dominant, is canceled. In contrast to negative feedback, it is a feed-forward technique and there are no stability issues. Noise canceling is a wideband technique and the principle does not rely on the use of inductors, which allows the implementation of compact receiver frontends. Furthermore, next to the noise canceling also distortion canceling was observed, possibly allowing the implementation of highly linear wideband frontends.

2.3.5 Noise canceling topologies

In the Thesis of F. Bruccoleri [11], also published with some extensions as a book [41], eight noise canceling topologies are presented and their performance is compared. The eight alternative noise canceling topologies (without biasing circuitry) are reprinted in Figure 2.5.

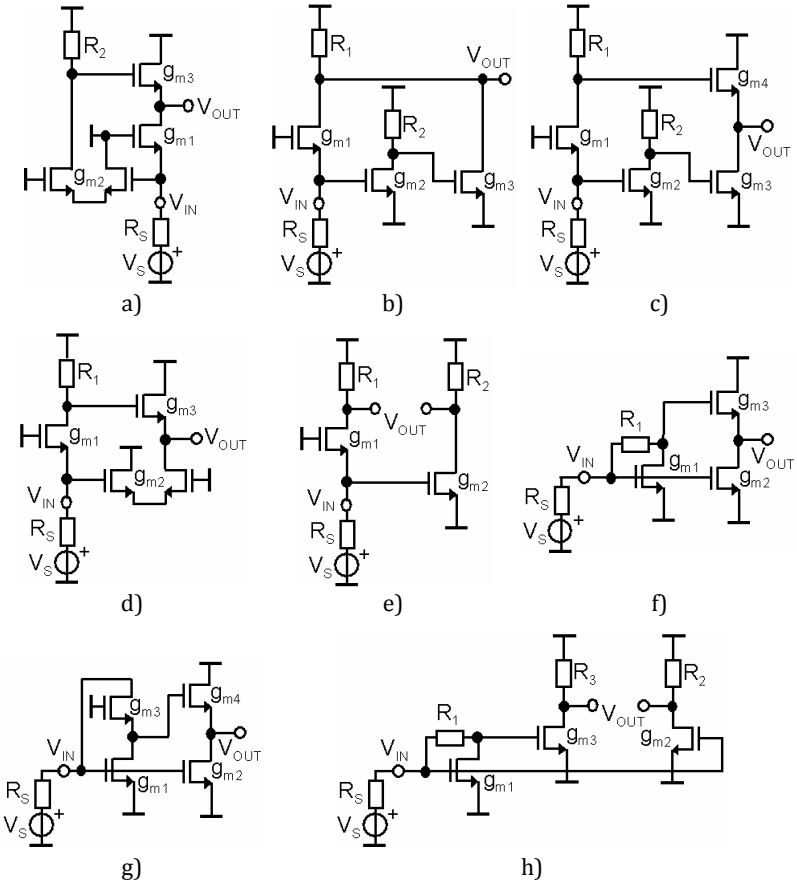

Figure 2.5: Alternative noise canceling topologies from Thesis F. Bruccoleri [11], biasing circuitry not shown.

For topologies a) to e) of Figure 2.5 the input impedance, which is typically equal to R_S, is determined by a transistor (g_{m1}) in common gate (CG) configuration[1]. In contrast to this, in topologies f), g) and h) the input transistor (g_{m1}) is in common source (CS) configuration,

[1] In common gate configuration, the *gate* terminal of the transistor is connected to a *common* node for in- and output, signal ground, this explains its name.

with its source terminal connected to signal ground. In these CS based topologies the output current of g_{m1} is fed back to its input via a resistor (R_1 in f) and h)) or transistor (g_{m3} in g)) in order to fix its input impedance.

The common source based noise canceling topologies (f), g), h)) use a form of negative feedback. However, there are important differences with the negative feedback technique described in section 2.3.3. First of all, the noise canceling topologies use local feedback around one transistor. Negative feedback topologies are often based on global feedback around two or more stages, which increases the risk of instability. Next to this, the noise canceling topologies have a direct relation between its input impedance and the transconductance of the input transistor (g_{m1}). To obtain a matched input impedance the transconductance needs to be: $g_{m1} = 1/R_S$. The noise of this transistor is canceled in noise canceling topologies. In negative feedback topologies, the noise of the input transistor is not canceled. Instead, low noise is obtained by using a transistor with high transconductance whereas the input impedance is set by (circuit elements in) the feedback loop.

Figure 2.6 shows the calculated noise figure of the topologies versus normalized power, neglecting biasing noise. The power is normalized on the power consumption of a common source stage with a transconductance equal to one over the source impedance ($g_m = 1/R_S$). Neglecting the noise from bias circuitry, 'Topology e)' shows the best noise performance.

Figure 2.7 shows the noise figure of the topologies taking the noise from biasing circuitry account, for two different supply voltages. The biasing noise is assumed to be inversely proportional to the available voltage headroom. Higher voltage headroom for the biasing circuitry results in lower biasing noise. 'Topology e)' still shows the best noise performance for high supply voltages ($V_{DD} = 3$ V) [1] and relatively low normalized powers ($\eta_{LNA} < 10$). For a lower supply voltage ($V_{DD} = 1.8$V),

[1] The comparison was made based on a ~0.3µm CMOS process, where $V_{DD} = 3$ V is a realistic option.

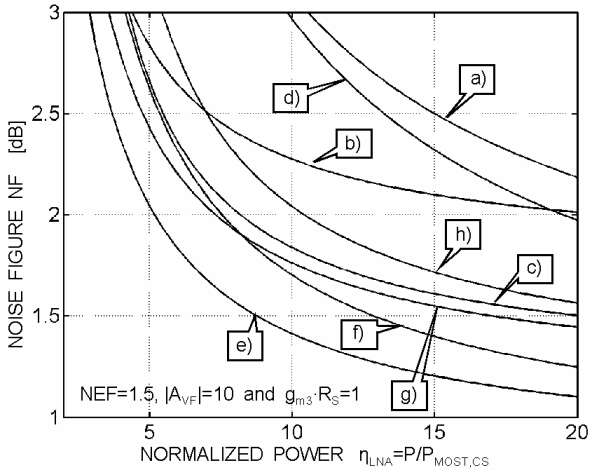

Figure 2.6: Noise figure of the noise canceling topologies versus normalized power (Figure 4.23 of [11]).

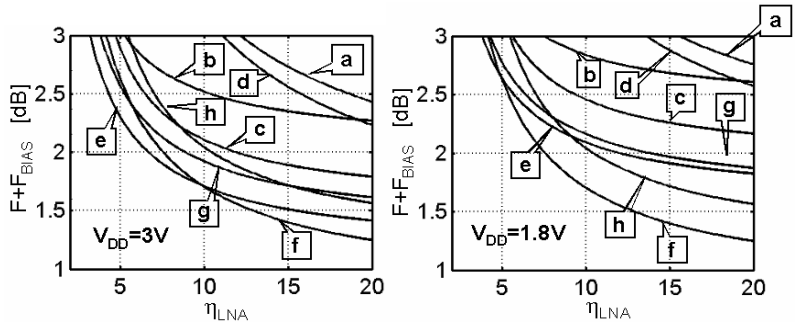

Figure 2.7: Noise figure of the topologies including biasing noise versus normalized power, for V_{DD}=3V and V_{DD} = 1.8V (Figure 4.26 of [11]).

'topology f)' has the lowest noise figure. However, for low normalized powers ($\eta_{LNA} < 5$), the difference in noise figure of 'topology f)' and 'topology e)' is negligible.

From the comparisons in Figure 2.6 and 2.7, two topologies stand out, 'topology e)' and 'topology f)'. 'Topology f)' was used for the low noise amplifier published in [39-40]. In contrast to 'topology f)', 'topology e)' has a differential output. The noise of the impedance matching (common gate) transistor is exactly canceled when the gain to both outputs are equal in magnitude. The single ended input signal is then converted into a balanced differential output signal, essentially implementing a balun. This is a very useful property for a wideband receiver of this topology as it saves the use of an external wideband (lossy) balun.

Because of its simple structure, noise performance and balun functionality, 'topology e)' was selected for further exploration and served as basis for the three designs discussed in Chapter 3, 4 and 5. As 'topology e)' consists of a common gate and a common source stage, it is referred to as the 'CG-CS topology.' This topology serves as the basis for the CG-autotrafo-CS LNA presented in Chapter 3. In Chapter 4 the focus is more on the balun functionality of the CG-CS topology, hence the name Balun-LNA is used. Furthermore, the BLIXER, a wideband receiver topology, presented in Chapter 5 is also based on the CG-CS topology.

2.4 Conclusions

The specifications on gain, noise figure and input impedance of a wideband receiver lie in the same order as for a narrowband receiver. However, in a wideband receiver these specifications need to be met over a bandwidth that is one or two orders of magnitude larger, in the order of a few gigahertz.

The third order linearity (IIP3) of a wideband receiver needs to be at least as good as in a narrowband receiver, preferably better. A wideband receiver has more requirements on second order nonlinearity than a narrowband receiver. In the mixer of a receiver there are sources of second order nonlinearity that are present in both narrow and wideband receivers, characterized by the 'RF-to-IF IIP2'. In a wideband receiver there is an additional requirement on the second order linearity of the gain in front of the mixer (RF-gain). In a wideband receiver the non-linearity of the RF-gain is

the dominant source of second order intermodulation distortion ('RF-to-RF IIP2'). Obtaining wideband receivers with high linearity is important, as pre-filters may be removed or their specifications relaxed. This in turn will result in more flexible and low-cost systems.

To allow battery operation, the power consumption of a wideband receiver must be kept low, in the same order as a narrow band receiver. Furthermore, for low-cost systems compact, inductor-less, circuit topologies are desired. In this thesis the aimed circuit specifications for the implementation of compact wideband receiver frontends are:

- RF-bandwidth in the order of a few gigahertz, covering as much as possible of the communication bands up to 10 GHz.
- Input impedance: 50 Ω
- Voltage gain of frontend: 20 dB[1]
- Noise Figure: < 5 dB
- IIP3: 0 dBm
- IIP2: +20 dBm (RF-to-RF)
- Power consumption in the order of tens of milliwatts
- Topologies with minimum number of inductors preferred

These specifications ask for new circuit topologies that are suitable to implement compact wideband receivers. Two wideband circuit techniques available at the start of this project (2004), distributed amplifiers and 'input-filter' based topologies, are not suitable for *compact* wideband receivers as these rely on the use of multiple integrated inductors.

At the start of the project negative feedback was seen as a possible candidate for compact wideband receivers. As it is a very well-known technique much research on this topic was to be expected. This research, assisted with the increasing f_T of newer CMOS generations, was likely to solve the issues of negative feedback, such as the risk of instability and high power consumption.

[1] Either RF-to-RF gain, for a traditional LNA-mixer having voltage gain at RF, or RF-to-IF gain, in case voltage gain is created at IF, see Chapter 5.

We opted to do research in a on another, still largely unexplored technique: the noise canceling technique. Based on the research of F. Bruccoleri, a particular interesting topology, 'topology e)' or the CG-CS topology, was selected. This topology achieves wideband noise canceling, has a single-ended input and a differential output, essentially integrating a wideband balun and LNA into one circuit. This topology serves as basis for the designs of Chapter 3-5.

Chapter 3

A wideband LNA using an on-chip transformer

This chapter was published at the Radio Frequency Integrated Circuits Symposium in June 2006 [14].

3.1 Introduction

Triggered by multi-standard radios and the upcoming Ultra Wideband standards, the interest in broadband receiver techniques has increased over recent years. A number of different CMOS LNAs combining a wideband input-match and gain have been proposed. To compensate for capacitive effects, several inductors are often used [29, 42-44]. Especially in nano-scale technologies inductors are considered expensive, as a complete microprocessor might fit in the same area. To reduce area, a promising wideband technique is the Noise Canceling (NC) technique, which in principle does not require any inductors [40]. In [40] a shunt-feedback LNA is designed and measured. An alternative single input, differential output NC-topology, consisting of a parallel operating Common Gate (CG) and Common Source (CS) stage, was also proposed, but not implemented. This paper reports results on this CG-CS LNA, just as recently done in [43]. However, whereas [43] uses 5 inductors, we only use a single on-chip transformer, which takes about the same area as a single inductor. Moreover, this transformer is exploited to the maximum, by using it simultaneously for biasing, source-impedance matching and for noiseless, powerless, voltage amplification. Section 3.2 describes how

the NC technique can be applied to a CG-stage. The evolution from the basic idea to a complete implementation is presented in section 3.3. Measurement results and a comparison to previous work are given in section 3.4. Finally, the conclusions are drawn in section 3.5.

3.2 The noise canceling technique applied to a common gate input stage

The CG-stage is well known for its wideband input match, and can realize wideband gain via a drain resistance (R_{CG}). Neglecting feedback from the drain, the minimum NF of a CG-stage matched to a source impedance is limited to about 4 dB, assuming a Noise Excess Factor (NEF = γ / α) of 1.5 for sub-micron CMOS processes. For a number of broadband standards, this NF is low enough to implement a receiver with acceptable sensitivity, provided one can realize enough gain to reduce the noise contribution of later stages. However, the transconductance (g_m) of the CG-stage is fixed by the matching, while the next stage determines the capacitive load. As a result, only the resistance R_{CG} remains as a design variable, and a trade-off between gain (high R_{CG}) and bandwidth (low R_{CG}) exists.

To remove this trade-off between gain and bandwidth – that is, to increase the gain while maintaining the same bandwidth – a second-stage can be added. A disadvantage is that such an additional amplifier will generate noise and consequently degrade the NF of the complete LNA-circuit. However, as shown in [40] the additional amplifier can be used to cancel the noise of the CG-stage. By applying the NC technique, the gain-bandwidth of the LNA can be increased while maintaining a low overall NF. Figure 3.1 shows this technique conceptually.

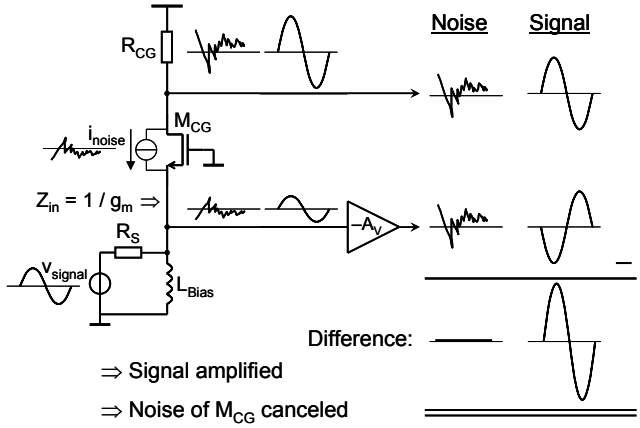

Figure 3.1: The Noise Canceling Technique applied to a CG-stage.

Assuming impedance matching, half of the noise generated by the CG-transistor (i_{noise}) flows via R_S to ground and generates a voltage variation at the source of M_{CG}. The same current necessarily has to flow via R_{CG} and will lead to voltage variation at the drain of M_{CG} (see Figure 3.1). These two noise-voltages at drain and source are fully correlated, as they have a common origin (i_{noise}), and are in anti-phase. In contrast, the voltages resulting from v_{signal} at the source and drain are in-phase. This property is exploited in the Noise Canceling Technique. The voltage at the source, a sum of noise and wanted signal, is amplified ($-A_V$) and subtracted from the voltage at the drain. As indicated in Figure 3.1, the noise is canceled because two correlated voltages with equal amplitude are subtracted. However, the wanted signal will increase in amplitude. This is because the wanted voltage at the drain of M_{CG} and at the amplifier (A_V) output, are combined in a constructive manner. The amplifier will clearly also generate noise, how to design a low-noise implementation will be discussed in the next section.

The required voltage gain of the voltage amplifier ($A_{req} = -A_V$) is easily calculated. A part (say α) of the noise, generated by i_{noise}, will leave transistor. This factor α depends on the source match; $\alpha = ½$ for perfect source matching. However, its value is not relevant in the calculation of A_{req}. The noise resulting from i_{noise} is canceled when the

resulting noise-voltage at the output of the voltage amplifier ($v_{noiseAV}$) is equal to the noise-voltage at the output of the CG-stage ($v_{noiseCG}$):

$$\begin{aligned} v_{noiseAV} &= v_{noiseCG} \\ \alpha \cdot i_{noise} \cdot R_S \cdot A_{req} &= \alpha \cdot i_{noise} \cdot R_{CG} \\ \Rightarrow \quad A_{req} &= \frac{R_{CG}}{R_S} \end{aligned} \tag{3–1}$$

Equation (3–1) shows that the required voltage gain is equal to the ratio of the common gate resistor and the source resistance. The input impedance of the CG-stage equals $1/g_{mCG}$. When the source is matched, this is equal to the source resistance: $R_S = 1/g_{mCG}$. The required gain can now be expressed as:

$$A_{req} = \frac{R_{CG}}{R_S} = \frac{R_{CG}}{1/g_{mCG}} = g_{mCG} \cdot R_{CG} = A_{V,CG} \tag{3–2}$$

From equation (3–2) , the following conclusion can be drawn: the noise canceling condition is met (for a matched input impedance) when the gain of the voltage amplifier equals the voltage gain of the CG-stage. This is a highly desirable property, since source-matching, noise-canceling, and balun-like operation can be obtained simultaneously.

3.3 Evolution of the implemented LNA

From the basic principle, described in the previous section, to a fully implemented circuit, requires a number of steps and decisions. This section describes how the original idea has evolved into the final circuit.

First of all, the CG-stage needs to be biased. A low-noise method of biasing the CG-stage is using an inductor between the transistor source node (CG-input) and ground (as shown in Figure 3.2; top left). An additional advantage is that there is no DC-voltage drop across the inductor. The voltage headroom available for the CG-stage is thus

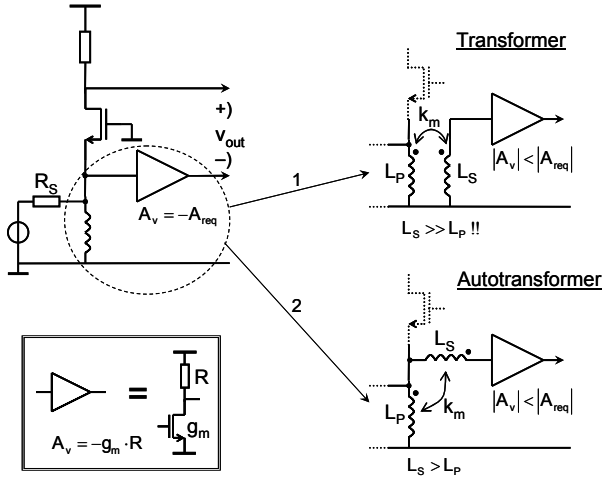

Figure 3.2: Alternatives for the implementation of the voltage amplifier A_V.

maximized by using an inductor, which is important – especially to achieve high gain at low supply voltages (high voltage drop across R_{CG}). An on-chip inductor will be used for this purpose, even though it occupies a large area compared to the active transistor area. Alternatively, if desired the inductor can easily be moved outside the chip.

As discussed in the previous section, Noise Canceling removes the output noise generated by the CG-transistor. The key to a low overall NF has now shifted to a low-noise implementation of the inverting voltage amplifier ($-A_V$). The most elementary implementation is a resistively loaded Common Source (CS) stage (Figure 3.2; bottom left). The transconductance (g_m) of this stage should be chosen to be as high as possible, in order to minimize the NF. However, the maximal achievable gm is limited by biasing and power consumption constraints.

The top right of Figure 3.2 shows an alternative to the simple CS-implementation of the voltage amplifier. This configuration exploits the principle that an ideal transformer realizes a noiseless voltage

gain at zero power consumption. Such a transformer can be created by inter-twining two inductors. Because an inductor is already present at the source of the CG-stage, this intertwined transformer will demand only a slight increase in area. The voltage amplifier behind the transformer isolates the output from the input and can still be implemented with a CS-stage. Due to the voltage amplification of the transformer, the requirements placed on the CS-stage are now reduced in two ways: (1) the voltage amplification of the CS-stage can be reduced; and (2) the transconductance (g_m) can be lowered since its noise contributes now less to the overall NF.

The voltage amplification of the transformer should be maximized in order to minimize the noise contribution of the CS-stage. The voltage amplification of a transformer is given by: $A_{V,trans} = k_m \cdot \sqrt{L_S / L_P}$, with k_m the magnetic coupling between primary and secondary windings and L_P and L_S their respective inductances. Typically, a k_m of 0.75 – 0.9 is attained for on-chip transformers [45].

To assess the feasibility of such a transformer, a modest transformer voltage amplification of 2 (6 dB) is assumed. For $A_{V,trans}$ = 2, it follows that L_S should be 5–7 times larger than L_P. These ratios are, in principle, realizable; however, wideband matching constraints put a limit to the minimum acceptable inductance of L_P. This results in a high inductance of L_S, which is accompanied by a too low self-resonance frequency (more specifically: $f_{selfres}$ < 10 GHz for multi-GHz operation), which in turn will impair the intended operation of the transformer.

However, an auto-transformer configuration requires much less inductance in the secondary winding for the same voltage gain than a traditional transformer. This configuration is shown at the bottom-right of Figure 3.2. By stacking the primary and secondary windings, the required ratio L_S/L_P is reduced. The voltage amplification of the autotransformer is given by: $A_{V,auto} = 1 + k_m \cdot \sqrt{L_S / L_P}$. When again a voltage gain of $A_{V,auto}$ = 2 is assumed, the required ratio L_S/L_P is reduced to only 1.2 – 1.8, using the previously assumed k_m-range. This reduction of roughly 4 times of L_S/L_P (from 5 to 1.2) makes it feasible to design a circuit suitable for multi-GHz operation.

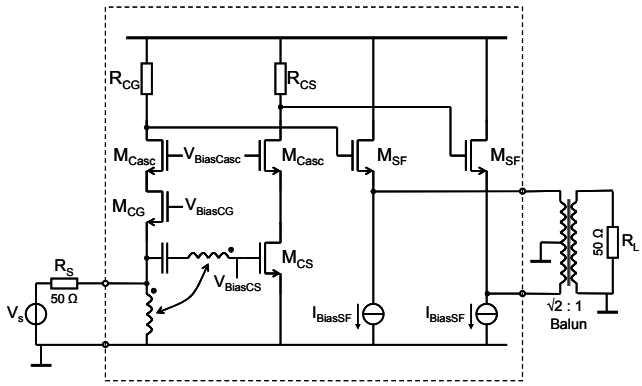

Figure 3.3: Simplified schematic of the complete LNA.

The implemented LNA is shown in Figure 3.3. The part within the box is integrated in a standard digital 90nm CMOS process. The balun at the output converts the differential 100Ω output impedance of the LNA into a single-ended 50Ω for measurement purposes. In the circuit, cascode transistors are used to improve the gain and reverse isolation. A symmetric, low-ohmic output is created by the source followers, which do not load the CG- and CS-stages too much.

The circuit is capable of driving a mixer directly and performs a single-ended to differential conversion. An external balun at the input is thus not needed, which gives a fundamental advantage in system NF. The loss of an input balun (1–2 dB) would add up directly to the total NF. The effective inductance of the transformer, mainly determined by L_P, resonates with the effective capacitance at the input. An acceptable S_{11} over a broad frequency-range is obtained by keeping the parasitic capacitance as low as possible, which results in a low-Q parallel RLC-section.

The die photo of the LNA is shown in Figure 3.4. The transformer – consisting of two intertwined inductors – is clearly visible. The single-ended G-S-G input pads are located on the top, while the differential G-S-S-G output pads can be found at the bottom. The five pads at the left side are used to supply and bias the circuit.

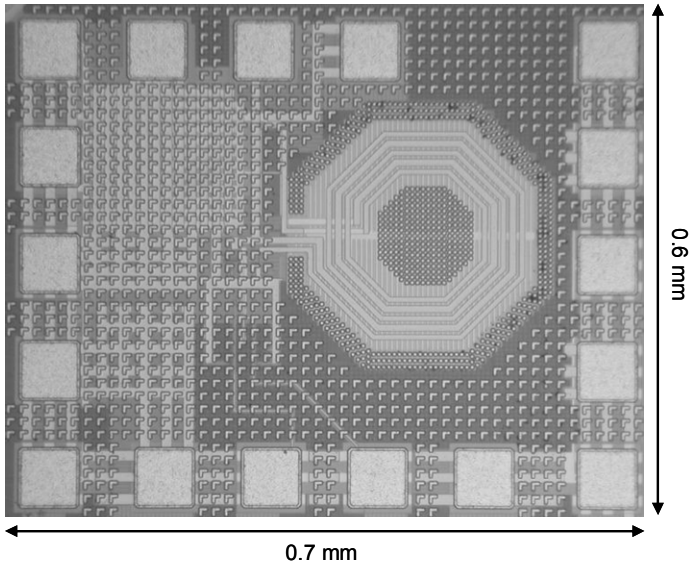

Figure 3.4: Die photo of the CS-autotrafo-CG LNA.

The chip size measures 0.6 × 0.7 mm, whereas the active area – without pads– covers an area of only 0.2 μm^2. Metal tiles cover a major part of the die to fulfill density rules.

3.4 Measurements and comparison

The measured S-parameters and Noise Figure are shown in Figure 3.5. The S_{11} dips below –10 dB from 2.5–4.0 GHz. In this frequency range the S_{21} is above 10 dB, and the NF is lower than 5.4 dB, with a minimum of 4.0 dB at 3.3 GHz. The S_{12} is under –40 dB from 1–8 GHz (not shown) and S_{22} is below –15 dB over the complete 1–10 GHz range.

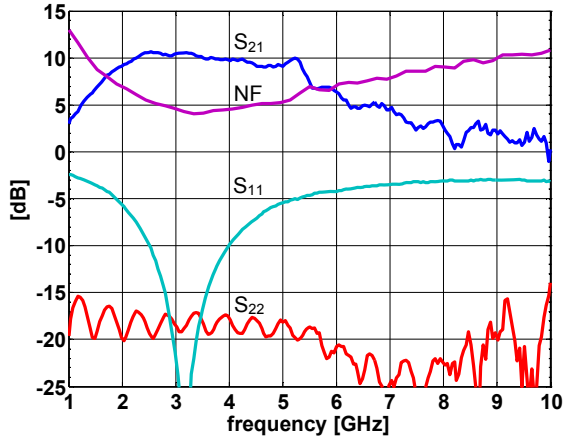

Figure 3.5: Measured S-parameters and Noise Figure.

The voltage gain of the LNA is the relevant gain when it is followed by an integrated mixer with a voltage input. The S_{21} of 10 dB translates, in this case, into a voltage gain of 19 dB, due to the single-ended to differential nature of the LNA: to account for the matched output 6 dB needs to be added, and an additional 3 dB is required to take the conversion from 50 Ω input- to 100 Ω differential output-impedance into account.

Table 3-I gives an overview of recently published wideband CMOS LNAs. Clearly, this design achieves the highest gain, consumes the least power and occupies the lowest chip-area. The NF is acceptable considering that the large voltage gain of the LNA will lead to minimal noise contributions of stages following the LNA. Next to this, a balun with its associated losses is also not needed.

TABLE 3-I
OVERVIEW OF RECENTLY PUBLISHED WIDEBAND CMOS LNAS

Parameter	[42] 2003	[29] 2004	[43] 2005	[44] 2005	This design
S11 [dB]	< -8	< -9.9	< -10	< -9	< -10
$S21_{max}$ [dB]	8.1	9.3	10 [1)]	9.8	10.6
BW [GHz]	0.6 – 22	2.3 – 9.2	0.1 – 6.5	2.4 – 4.6	2.5 – 4.0
NF [dB]	4.3 – 6.0	4.0 – 9.0	3 – 4.2	2.3 – 4.0	4.0 – 5.4
IIP3 [dBm]	-	-6.7	+1 [2)]	-7	-8
Topology	Distri-buted	LC-filter based	Noise canceling + LC-filter	Inductive degen. + res. shunt feedback	Noise canceling + trans-former
Technology	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	90 nm CMOS
Power core [mW] (total)	52	9 (18)	12	12.6 (16.2)	8 (16)
# inductors	8	5	5	3 [3)]	1
Area [mm2] (excl.pads)	~0.7	~0.5	~0.4	~0.4	0.2

[1)] Article reports 19 dB voltage gain
[2)] Simulated value
[3)] 2 off-chip inductors.

3.5 Conclusions

Based on the Noise-Canceling Technique a new single-ended-input–differential-output LNA topology is presented, which exploits an on-chip transformer. The transformer is used to tune out the capacitance at the input, and realizes a passive, power-free, low-noise voltage gain.

The resulting LNA achieves a high voltage gain of 19 dB, a broadband input match (2.5 – 4.0 GHz) and a noise figure of 4.0 – 5.4 dB at a core power consumption of 8 mW. It is the smallest broadband LNA in the multi-GHz range published so far and it requires no external components.

Chapter 4

An inductorless wideband Balun-LNA

This chapter was published in the IEEE Journal of Solid-State Circuits of June 2008 [16].

4.1 Introduction

Upcoming software-defined and multi-standard radio architectures may cover all major communication bands in use today up to 6 GHz [20]. This puts interesting demands on the radio and its low noise amplifier (LNA). The wanted frequency span can be chopped into smaller bands which then can be processed by several dedicated, possibly tuned, LNA circuits. The other extreme is a single LNA, which then obviously needs to have large bandwidth. In contrast to a multi-LNA solution, the single wideband LNA is flexible and efficient in terms of area, power and costs. Single-ended input LNAs are preferred to save I/O pins and because antennas and RF filters usually produce single ended signals. On the other hand, differential signaling in the receive chain is preferred in order to reduce second order distortion and to reject power supply and substrate noise. Thus, at some point in the receive chain a balun is needed to convert the single-ended RF signal into a differential signal. Off-chip baluns with low losses are typically narrowband so that several baluns would be required in case of wideband operation. On the other hand, wideband passive baluns typically have high loss, degrading the overall NF of a receiver significantly.

Combining the balun and LNA functionality into a single integrated circuit seems an attractive option to realize a wideband low noise receiver front-end. However, only a few CMOS wideband LNA-balun combinations with sufficient low noise figure for multi-band receivers (3–4 dB) have been published [14, 20, 43]. These circuits all exploit the noise canceling topology published in [[40], Fig. 4b], shown in Figure 4.1. This is one of the noise canceling topologies discussed in [41]. Although these circuits have a single-ended input and differential output, the (im)balance of the output signal is not reported. We will show that this imbalance can be significant, e.g. about 6dB in [[20], Fig. 8a]. Next to this, the circuits in [14, 20, 43] all use integrated inductors. As in newer CMOS technologies the area-costs increase, area-consuming integrated inductors become increasingly expensive. Finally, we prefer to use baseline transistors at the standard supply voltage of 1.2V instead of thick oxide transistors at 1.8V [43] or 2.5V supply [20]. This is challenging with respect to achieving sufficient gain and good linearity.

In this paper we present an inductorless Balun-LNA with a well-balanced output signal, and will show that it can achieve wideband amplification at low noise in a baseline 65nm CMOS process with standard 1.2V supply voltage, while also achieving good linearity. The measurements on this circuit were published in [15]. This paper gives an in-depth analysis of the design options, the noise behavior and distortion behavior of the used circuit topology. Furthermore, to the authors' knowledge, this is the first paper in which it is recognized that cross-terms in the $I_{DS}(V_{GS}, V_{DS})$ characteristic of modern sub-micron CMOS transistors can be exploited to obtain an amplifying stage with low second order distortion.

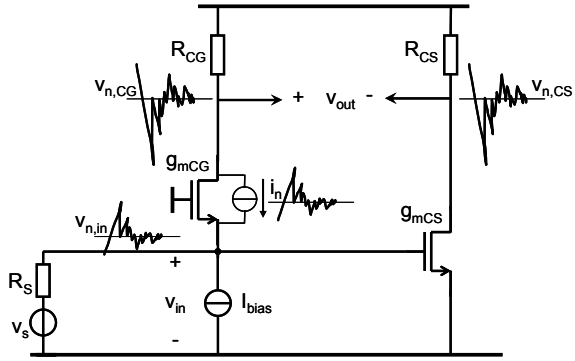

Figure 4.1: The basic Common Gate - Common Source topology in which the noise of the CG-transistor can be canceled.

The Balun-LNA circuit topology is depicted in Figure 4.1. This Common Gate (CG) stage in parallel to a Common Source (CS) stage is a well-known structure. Actually, there are at least 15 to 20 year old references [46] and [[47], Figure 2 and 3], and possibly even older ones. Later, this structure has been used in the "MICRO-MIXER" circuit [48] and the LNA in [20]. However, all these circuits use CG and CS devices with identical size and bias. As will be shown in section 4.2 and 4.3, identical devices cannot simultaneously bring the benefits of output balancing, noise canceling and distortion canceling.

This paper provides insight in circuit dimensioning trade-offs and reveals new ways to exploit the circuit to maximize performance. To this end, section 4.2 derives conditions for simultaneous output balancing, noise canceling and distortion canceling. Section 4.3 details the noise analysis and motivates why appropriate scaling of the CS-stage is needed to exploit noise canceling most effectively and obtain a noise figure in the order of 3 dB or lower. Apart from noise, the circuit also simultaneously renders distortion canceling of the (CG-) matching-device nonlinearity [40]. However, to benefit from this, the CS-stage needs to have low distortion too. Therefore, we analyze distortion in detail in section 4.4, focusing on short channel devices. The distortion generated by these devices is not only due to non-linearity of their transconductance (g_m) and of their output

conductance (g_{ds}), but also due to the dependence of gm on the drain-source bias voltage. We will show that a (cross-) term describing this dependence can be used to cancel the dominant 2nd order distortion due to g_m. Together with the distortion canceling of the CG-stage this results in a high overall IIP2. In section 4.5 we describe the actual Balun-LNA circuit design, to validate theory and set an expectation for the measurements. Section 4.6 presents measurements and benchmarks the LNA to previous designs, while section 4.7 presents the summary and conclusions.

4.2 Simultaneous balancing, noise and distortion canceling

In the sections below we will briefly derive the conditions for simultaneous balancing, noise canceling and distortion canceling. We will neglect capacitive effects for simplicity, and verify the validity of this assumption later via measurements. A more detailed discussion on high frequency limitations and robustness for component variations can be found in [41].

4.2.1 Balancing (balun operation)

The Common Gate stage in Figure 4.2, biased with a current source, has a straightforward relation between its voltage gain ($A_{v,CG}$) and its input impedance ($R_{in,CG}$). The signal current (i_{Rcg}) flowing through the load resistor R_{CG} has to be equal to the signal current flowing at the input (i_{in}), as there is no alternative path to ground. Thus,

$$i_{in} = i_{Rcg} = \frac{v_{out,CG}}{R_{CG}} = \frac{v_{in} \cdot A_{v,CG}}{R_{CG}} \tag{4–1}$$

As a result, the input impedance of the CG-stage can be expressed as:

$$R_{in,CG} = \frac{v_{in}}{i_{in}} = \frac{R_{CG}}{A_{v,CG}} \tag{4–2}$$

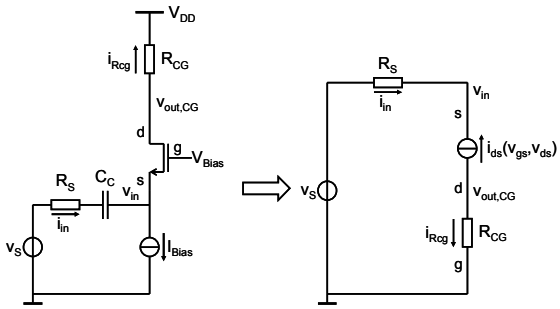

Figure 4.2: Small signal equivalent of a CG-stage.

For an ideal transistor, having infinite output resistance, this is obvious. In that case the input impedance can be written as $R_{in,CG} = 1/g_m$ and the gain equals $A_{v,CG} = g_m \cdot R_{CG}$. However, (4–1) and (4–2) are equally valid when the finite output resistance and the body-effect of a real transistor are taken into account.

For an impedance match at the input, the input impedance of the CG-stage ($R_{in,CG}$) should equal the source resistance (R_S), thus the gain of the CG stage becomes:

$$A_{v,CG} = \frac{R_{CG}}{R_{in,CG}} = \frac{R_{CG}}{R_S} \tag{4–3}$$

To create a balun, the gain of the CS-stage in Figure 4.1 should be equal, but have opposite sign, thus:

$$A_{v,CS} = -A_{v,CG} = -\frac{R_{CG}}{R_S} \tag{4–4}$$

4.2.2 Noise canceling

The noise generated by the CG-transistor in Figure 4.1 can be represented by a current source (i_n). This current generates both a voltage at the input-node ($v_{n,in} = \alpha_1 \cdot i_n \cdot R_S$) and a fully correlated anti-phase voltage at the CG-output ($v_{n,CG} = -\alpha_1 \cdot i_n \cdot R_{CG}$). The factor α_1 equals the

voltage division between the input resistance ($R_{in,CG}$) and the source resistance (R_S), which equals in case of impedance matching:

$$\alpha_1 = \frac{R_{in,CG}}{R_{in,CG} + R_S} \tag{4–5}$$

The noise at the CS-output equals the CG-output noise ($v_{n,CS} = v_{n.in} \cdot A_{v,CS} = v_{n,CG}$), when the CS-gain $A_{v,CS}$ satisfies (4–3). Thus, the noise contribution of the CG-transistor can be canceled, as it becomes a purely common-mode signal at the differential output (v_{out}). This proofs that simultaneously balancing of the output signal and noise canceling is obtained.

4.2.3 Distortion canceling

As derived in [40], not only the noise of the impedance matching device is canceled, but also its non-linearity, assuming it can be modeled as a current source between drain and source, controlled by the gate-source voltage. We will take this one step further here, by also taking into account the influence of the drain-source voltage on the drain current. This allows the modeling of the non-linear output conductance and other 2nd-order effects like Drain Induced Barrier Lowering (DIBL), which become more prominent in modern CMOS processes.

Figure 4.2 on page 47 shows a model of the CG-stage. Weakly nonlinear behavior is assumed, modeled by a drain-source current ids which depends non-linearly on both voltage variations v_{gs} and v_{ds} around their DC bias points . The source signal (v_s) causes a non-linear drain-source current (i_{ds}) which is converted into a non-linear voltage at the input (v_{in}) via the (linear) source resistor R_S. The non-linear input voltage (v_{in}) can be written as a Taylor expansion of the signal source voltage (v_s):

$$\begin{aligned} v_{in} &= \alpha_1 \cdot v_s + \alpha_2 \cdot v_s^2 + \alpha_3 \cdot v_s^3 + \alpha_4 \cdot v_s^4 + \ldots \\ &= \alpha_1 \cdot v_s + v_{NL} \end{aligned} \tag{4–6}$$

where the α's represent Taylor coefficients and v_{NL} contains all unwanted nonlinear terms and the first Taylor coefficient (α_1) is defined in (4–5).

The output voltage of the CG-stage (see Figure 4.2) can be written as:

$$\begin{aligned} v_{out,CG} &= i_{in} \cdot R_{CG} = \frac{v_s - v_{in}}{R_S} \cdot R_{CG} \\ &= \left((1-\alpha_1) \cdot v_s - v_{NL} \right) \frac{R_{CG}}{R_S} \end{aligned} \tag{4–7}$$

where (4–6) is used. The output voltage of the CS-stage can be written using (4–4):

$$v_{out,CS} = -v_{in} \frac{R_{CG}}{R_S} = -\left(\alpha_1 \cdot v_s + v_{NL}\right) \frac{R_{CG}}{R_S} \tag{4–8}$$

The difference in sign of the wanted signal v_s and unwanted signal v_{NL} in (4–7) and (4–8) can be exploited: after subtraction only the linear signal remains:

$$v_{out,diff} = v_{out,CG} - v_{out,CS} = v_s \cdot \frac{R_{CG}}{R_S} \tag{4–9}$$

In conclusion, all noise and distortion currents generated by the CG-transistor can be canceled, irrespective whether produced due to non-linearity of the transconductance or non-linearity of the output conductance. The gain required in the CS-stage to cancel the distortion products of the CG-transistor equals the gain required to obtain output balancing, leading to the conclusion that simultaneous balancing and cancellation of unwanted noise and distortion currents of the CG transistor is possible. As the distortion due to the CG-transistor is canceled, while R_{CG} is normally quite linear, the CS-stage will determine the overall linearity of the complete LNA. The linearity of the CS-stage will be analyzed in section 4.4.2. The final noise is determined by R_{CG} together with the CS-stage, as will be shown in the next section.

4.3 Noise analysis

In this section we analyze the Noise Figure of the basic CG-CS LNA (Figure 4.1) for three different design options. To simplify the calculation, transistors are assumed to have infinite output impedance and the bias current source of the CG-transistor is assumed to be ideal. Furthermore only the thermal noise of the resistors and of the transistors is taken into account assuming $\gamma = 2/3$, which is known to be optimistic for short channel devices. These assumptions will over-estimate the gain and under-estimate the NF. However, the calculation is useful to compare the different design options and simplifies comparison to previously published results using similar assumptions. The output noise power of the circuit elements in Figure 4.1 can be calculated, and divided by the noise contribution of the signal source, leading to the noise factor:

$$\begin{aligned} F = 1 &+ \frac{\gamma \cdot g_{mCG} \cdot \left(R_{CG} - R_S \cdot g_{mCS} \cdot R_{CS}\right)^2}{R_S \cdot A_V^2} \\ &+ \frac{\gamma \cdot g_{mCS} \cdot R_{CS}^2 \cdot \left(1 + g_{mCG} \cdot R_S\right)^2}{R_S \cdot A_V^2} \\ &+ \frac{\left(R_{CG} + R_{CS}\right) \cdot \left(1 + g_{mCG} \cdot R_S\right)^2}{R_S \cdot A_V^2} \end{aligned} \qquad (4\text{–}10)$$

where the 2nd part is the contribution from the CG-transistor, the 3rd part from the CS-transistor and the last part from the load resistors, while the voltage gain (A_V) equals:

$$A_V = g_{mCG} \cdot R_{CG} + g_{mCS} \cdot R_{CS} \qquad (4\text{–}11)$$

Three different design options of the CG-CS circuit are now considered:

1) The transconductances of the CS and CG transistors are equal and the load resistors are equal, thus: $g_{mCS} = g_{mCG}$ and $R_{CS} = R_{CG}$ (the traditional way to implement an active balun [46], [47], using a CG-CS amplifier).

2) The transconductance of the CS transistor is *n* times bigger than the CG-transconductance and the load resistors are equal, thus: $g_{mCS} = n \cdot g_{mCG}$ and $R_{CS} = R_{CG}$ (design option used in [20]).

3) The CS-transconductance is n times bigger than the CG-transconductance and the CS-resistor is n times smaller than the CG-resistor, thus: $g_{mCS} = n \cdot g_{mCG}$ and $R_{CS} = R_{CG} / n$ (characterizes the design presented in this article).

The ratio of the voltage gain of the CS- and the CG-stage is defined as the gain imbalance:

$$\Delta A_V = 20 \cdot log\left(\frac{A_{V,CS}}{A_{V,CG}}\right) = 20 \cdot log\left(\frac{g_{mCS} \cdot R_{CS}}{g_{mCG} \cdot R_{CG}}\right) \qquad (4\text{–}12)$$

The Noise Figure, voltage gain (A_V) and gain imbalance (ΔA_V) of the three design options are plotted versus the impedance scaling factor *n* in Figure 4.3. In all three cases the CG-transconductance is assumed to be: $g_{mCG} = 1/R_S$, to have input impedance matching and $R_{CG} = 4 \cdot R_S$ to have a reasonable gain of the CG-stage.

Option 1) gives horizontal lines, as it does not depend on the factor *n*. The NF equals 3.4 dB, the voltage gain is 18.1 dB (= 8) and the output signal is perfectly balanced (ΔA_V = 0 dB). Although the noise of the CG-transistor is fully canceled, this effect is not exploited to achieve a NF below 3 dB. The noise generated by the CS-stage is significant because of its low transconductance ($g_{mCS} = 1/R_S$) and the voltage division of 1/2 by R_S and R_{in} magnifies its contribution.

Option 2) shows a decreasing NF and an increase in voltage-gain with increasing *n*. These two positive effects are however countered by an increase in gain imbalance. As *n* increases, the voltage gain of the CS-stage gain increases whereas the CG-voltage gain remains constant.

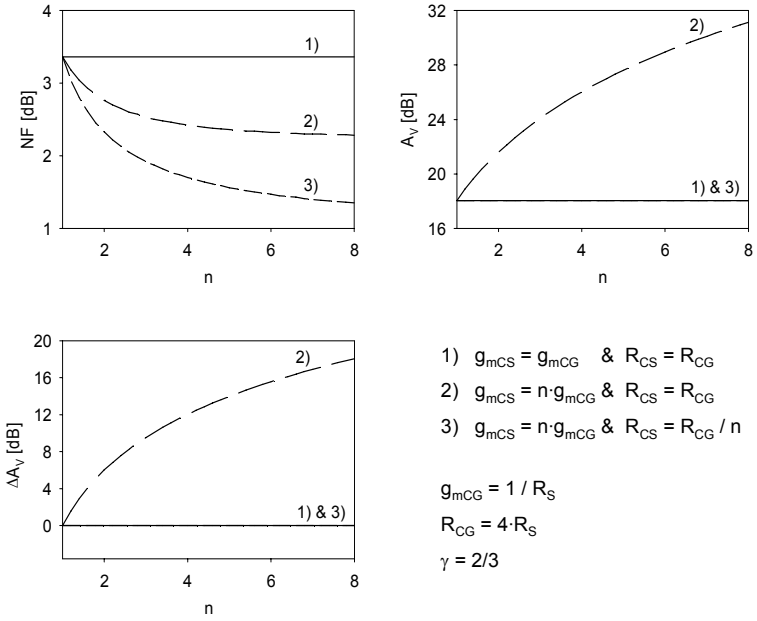

Figure 4.3: Noise figure (*NF*), voltage gain (A_V) and gain imbalance (ΔA_V) versus impedance scaling factor '*n*' for three different cases.

The last option, 3), shows an even faster decrease of NF than in option 2). In contrast to option 2), the noise of the CG-transistor is fully canceled. Next to this, the contribution of the CS-transistor decreases with a factor $1/n$ for increasing *n*, whereas in option 2) this contribution decreases at a rate slower than $1/n$. The voltage gain remains constant for option 3). Both the transconductance and the resistance of the CS-stage are scaled simultaneously (admittance scaling [49]). Thus the gain of the CS-stage remains constant and no gain imbalance occurs, i.e. the balun functionality is maintained for all values of *n*.

Now some more attention is given to design option 2) as published in [20]. Both in the calculation above and in [20] the load resistors have a value of $4 \cdot R_S$ (= 200 Ω). The transconductance-scaling factor in

[20] is estimated to be in the range $n = 2 – 3$, using the square-law MOS-model. This translates into a gain imbalance between CG- and CS-stage of 6 – 9.5 dB and (10) gives a NF between 2.8 and 2.5 dB. The remarkably low NF reported in [[20], Figure 8b] of about 2.2 dB is a simulation result where $\gamma = 1/2$ is assumed (instead of $\gamma = 2/3$, or higher) [50]. In the abstract of [20] a much higher NF of 3–3.5 dB is given.

Overall, we conclude that admittance scaling of the CS-stage (option 3) is the best way to achieve low noise figure in the order of 3 dB or below, while simultaneously achieving good output balancing. It is possible to get more gain using option 2 [20], but this comes at the cost of suboptimal noise behavior and significant imbalance in the output signal.

4.4 Linearity analysis

In this section we will analyze the nonlinearity of the Balun-LNA proposed in the previous section and see how we can exploit the distortion cancellation property. However, before we do so, we first want to introduce the IIP2 problem of wideband LNAs.

4.4.1 Linearity requirements for wideband receivers

Like a narrowband zero-IF or near zero-IF receiver, a wideband receiver is sensitive to the 2^{nd} order intermodulation product generated by an AM modulated carrier via AM detection. However, a wideband receiver may also suffer from 2^{nd} order intermodulation generated by interferers that have a sum or difference frequency equal to the wanted RF-input signal. The response to a modulated carrier can be suppressed by placing a high-pass filter (i.e. AC-coupling) between the LNA-output and mixer-input and by driving and designing the mixer in a well-balanced way [25]. However, the intermodulation product generated at a frequency equal to the frequency of the wanted signal cannot be separated from the signal. Especially standards that operate on large bandwidths, like DVB-H (470–862 MHz) [51] or WiMedia UWB (3.1–10.6 GHz) [12], have a high probability that a certain combination of interferers renders an in-band intermodulation product. A receiver designed for these

standards should have an LNA with sufficiently high IIP2 (and IIP3) in order to handle strong interferers like WLAN (IEEE 802.11a/b/g) and the GSM standards. The required intercept points depend strongly on the assumed interferer scenario and the assumed amount of pre-filtering of the interfering signals.

For a WiMedia UWB receiver the required IIP2 is above +20 dBm and IIP3 above –9 dBm as derived in [[24], Section II]. For a DVB-H receiver, consider a GSM interferer (1.8 GHz, +30 dBm at 0.2 m distance) and a WLAN interferer (2.4 GHz, +20 dBm at 1 m) that generate second order intermodulation product in the DVB-H band at 600 MHz. The received interferer power levels will be +7 dBm (GSM) and -20 dBm (WLAN). For a decrease in sensitivity of 3 dB, the maximum allowable interference level in a DVB-H receiver is -105 dBm [51]. Without filtering the required IIP2 would become: $IIP2 = P_{int1} + P_{int2} - P_{IM,max} = 7 - 20 + 105 = +92$ dBm(!). Assuming that both (out-of-band) interferers can be filtered with 35 dB attenuation brings the required IIP2 back to a more realistic value of +22 dBm.

4.4.2 Distortion of the CS-stage

As the distortion of the CG-stage can be canceled in the parallel CG- and CS-stage amplifier (section 4.2), the distortion performance of the total amplifier is determined by the distortion behavior of the CS stage. For distortion calculations often only the non-linearity of the transconductance of a transistor is taken into account. However, as in [52-53], we find that the non-linearity of the output conductance can not be neglected anymore in modern CMOS-processes. The drain current (i_{ds}) as function of the gate-source voltage (v_{gs}) and the drain-source voltage (v_{ds}) can be written as a 2-dimensional Taylor approximation:

$$\begin{aligned} i_{ds}(v_{gs}, v_{ds}) = \; & g_{m1}v_{gs} + g_{ds1}v_{ds} \\ & + g_{m2}v_{gs}^2 + g_{ds2}v_{ds}^2 + x_{11}v_{gs}v_{ds} \\ & + g_{m3}v_{gs}^3 + g_{ds3}v_{ds}^3 + x_{12}v_{gs}v_{ds}^2 + x_{21}v_{gs}^2v_{ds} + \ldots \end{aligned} \tag{4–13}$$

Where the Taylor coefficients can be derived from the large signal relations between I_{DS}, V_{GS} and V_{DS}:

$$g_{mk} = \frac{1}{k!}\frac{\partial^k I_{DS}}{\partial V_{GS}^k}$$
$$g_{dsk} = \frac{1}{k!}\frac{\partial^k I_{DS}}{\partial V_{DS}^k} \qquad (4\text{–}14)$$
$$x_{pq} = \frac{1}{p!q!}\frac{\partial^{p+q} I_{DS}}{\partial V_{GS}^p \partial V_{DS}^q}$$

Notice that in (4–13) i_{ds} not only depends on powers of v_{gs} and v_{ds} but also on cross-terms (x_{11}, x_{12}, etc.) of v_{gs} and v_{ds}. The cross-term x_{11} can be described as the dependence of the transconductance (g_{m1}) on the drain-source bias voltage. One of the reasons for this dependence is the DIBL-effect (Drain Induced Barrier Lowering). The terms x_{12}, x_{21}, etc. are higher order derivatives of x_{11}. The cross-terms will prove to be very important for the linearity in modern short-channel CMOS processes. In [54] the importance of these cross-terms was shown for MESFET transistors, which have linearity characteristics that are somewhat similar to MOSFETs. The linearity of a resistively loaded CS-transistor (g_{mCS} and R_{CS} in Figure 4.1) is calculated. The variation of the drain source voltage (v_{ds}) is set by the output current of the transistor (i_{ds}) and the load resistor R_{CS}. Using this and (4–13) v_{ds} can be expressed in a Taylor approximation of v_{gs}:

$$v_{ds} = c_1 v_{gs} + c_2 v_{gs}^2 + c_3 v_{gs}^3 + \ldots \qquad (4\text{–}15)$$

with the following Taylor coefficients:

$$c_1 = -g_{m1} \cdot \left(R_{CS} \;//\; (1/g_{ds1})\right)$$
$$c_2 = -\left(g_{m2} + g_{ds2} c_1^2 + x_{11} c_1\right) \cdot \left(R_{CS} \;//\; (1/g_{ds1})\right) \qquad (4\text{–}16)$$
$$c_3 = -\left(g_{m3} + g_{ds3} c_1^3 + 2 g_{ds2} c_1 c_2 + x_{11} c_2 + x_{12} c_1^2 + x_{21} c_1\right) \cdot \left(R_{CS} \;//\; (1/g_{ds1})\right)$$

To demonstrate the importance of the coefficients in (4–16), they have been derived from simulations. The circuit parameters of the

simulated CS-stage are: W/L = 300μm/0.06μm and R_{CS} = 50Ω. MOS model 11 [55], known for its accurate linearity modeling, is used for the transistor model. Figure 4.4 shows the drain-source current (I_{DS}) and the drain-source voltage (V_{DS}) versus the gate-source bias voltage (V_{GS}).

In the inset of Figure 4.5 the linear voltage gain (c_1) of the CS-stage versus V_{GS} is plotted. The second order coefficient c_2 is proportional to the derivative of c_1, thus it equals 0 at the maximum gain point (c_1 = -4 at $V_{GS} \approx$ 0.5 V). The three contributions that sum up to c_2 in (4–16) are also shown in Figure 4.5.

In the lower range of V_{GS}, where the transistor is in saturation, the 2nd order distortion due to the cross-term (x_{11}) is in the same order (but with opposite sign) as the 2nd order coefficient generated by the transconductance non-linearity (g_{m2}). These two terms cancel each other around the maximum in gain ($V_{GS} \approx$ 0.5V). The contribution due to the output conductance (g_{ds2}) in this V_{GS} range is small. As V_{GS} increases (and V_{DS} decreases) the transistor goes into linear operation, which results in lower transconductance non-linearity (g_{m2}). However, the output conductance nonlinearity (g_{ds2}) increases significantly above V_{GS} = 0.5V due to the decreasing V_{DS}. The contribution due to the cross-term remains relatively constant over a broad range of V_{GS} values.

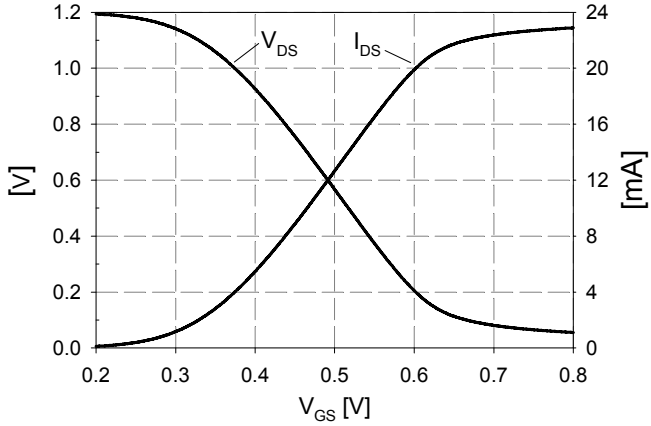

Figure 4.4: V_{DS} and I_{DS} versus V_{GS} of a resistively loaded CS-stage.

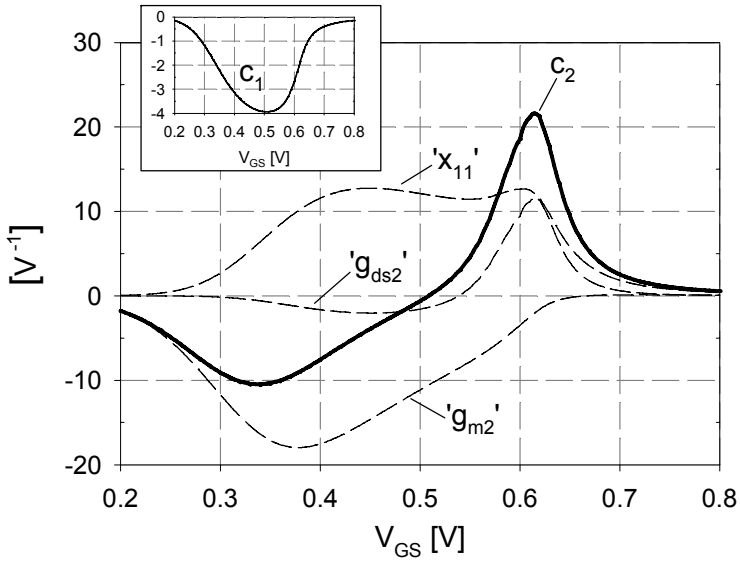

Figure 4.5: Simulated 2nd order non-linearity coefficient (c2) and individual contributions due to the transistor coefficients (gm2, gds2 and x11).
Inset: linear gain coefficient (c1) of the CS-stage.

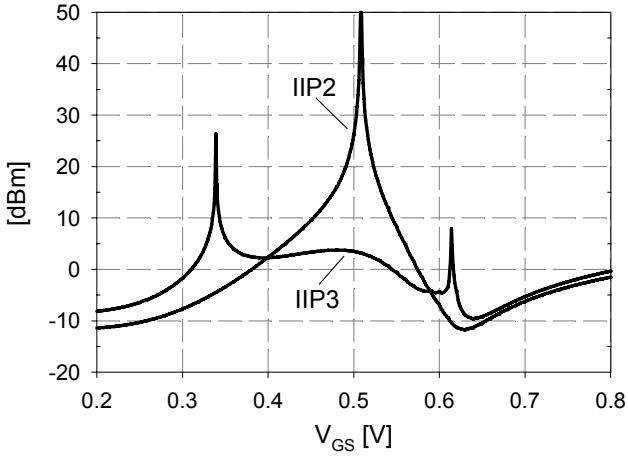

Figure 4.6: Simulated IIP2 and IIP3 of a resistively loaded CS-stage.

Figure 4.6 shows the IIP2 and IIP3 versus V_{GS} of the resistively loaded CS-stage. These graphs were derived from the Taylor coefficients c_1, c_2 and c_3 using:

$$IIP2_{dBm} = 20 \cdot log_{10}\left(\left|\frac{c_1}{c_2}\right|\right) + 10dB$$
$$IIP3_{dBm} = 20 \cdot log_{10}\left(\sqrt{\left|\frac{4}{3}\frac{c_1}{c_3}\right|}\right) + 10dB \qquad (4\text{–}17)$$

where the factor 10 dB accounts for the conversion from peak-voltage to power expressed in dBm, using an impedance level of 50 Ω. This shows that the resistively loaded CS-stage is capable of achieving an IIP2 higher than +20dBm with an IIP3 higher than +2dBm when it is biased close to the point where it reaches a maximum in gain.

4.5 Circuit design

Figure 4.7 shows the Balun-LNA circuit, the circuit inside the dashed box is implemented on silicon. The voltage gains of the CG- and CS-paths are designed to be equal, giving the balun function. However, the CS-stage is scaled up *n*-times by admittance scaling to achieve lower noise (see section 4.3). As a result the output impedance of the CG and CS-stage are not equal. To solve this, the outputs of both amplifier paths are buffered by identical source-followers, both having 50 Ω output impedance. These source-followers are currently also used as measurement buffers; in a complete receiver design they can drive a mixer, usually at a higher impedance level and reduced current.

To maximize balanced operation, the DC-levels at the gates of the source followers are chosen equal. This is achieved by AC-coupling the output of the CS-stage to its source-follower and generating the DC-level (V_{Repl}) by a scaled replica of the CG-stage (see Figure 4.7). The

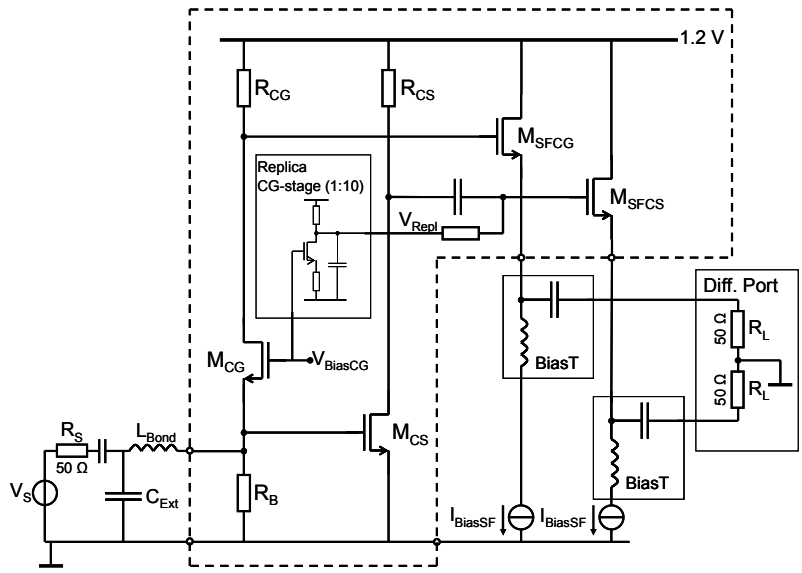

Figure 4.7: Schematic of the wideband Balun-LNA; the circuit within the dashed box is integrated on chip.

cut-off frequency of the AC-coupling is designed to be at 10MHz. This is more than a decade below the intended minimum operation frequency, which keeps the error in phase difference of the two paths within a few degrees of 180°. The transconductance of M_{CS} (g_{mCS}) is chosen 5 times higher than g_{mCG} to limit its noise contribution. The resistor R_B acts as a current source and is chosen 7 times higher than R_S, thereby limiting its noise contribution to about 0.3dB.

4.6 Measurements

The LNA, which has an active area of only 110µm × 80µm, has been fabricated in a baseline 65nm CMOS process and is mounted on a PCB, see Figure 4.8. For quick prototyping only the most critical connections for the RF performance, the in- and outputs, are bonded. The supply and bias are applied using a probe. By using adequate on-chip decoupling, the effects due to inductance in the supply lines are suppressed.

4.6.1 Gain, input-match and isolation

Figure 4.9 shows the measured single-ended input to differential output S-parameter gain, S_{ds21}. This parameter characterizes the gain of the LNA using a 50 Ω single-ended input port and a 100 Ω

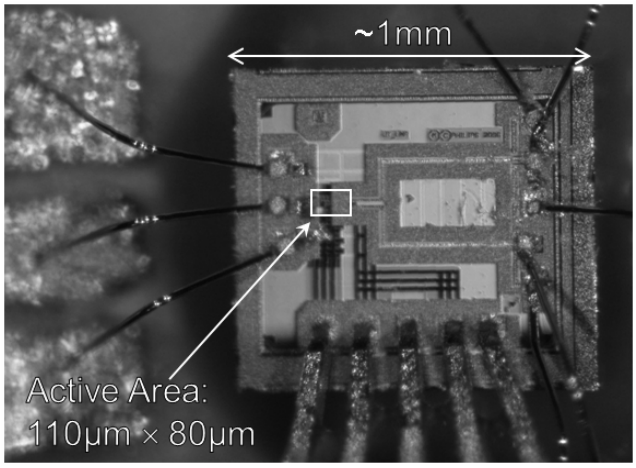

Figure 4.8: Die photo of the bonded wideband Balun-LNA.

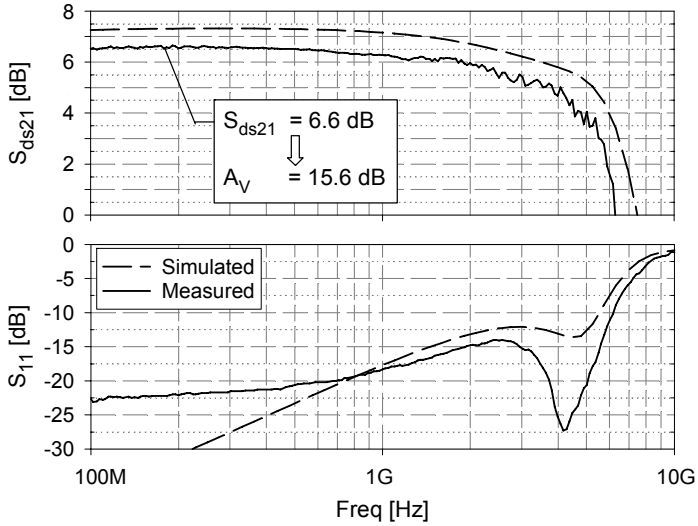

Figure 4.9: Simulated and measured S-parameters, S_{ds21} (Gain: single-ended in, differential out) and S_{11}.

differential output port. In practical use, the LNA will usually be followed by an on-chip mixer with a voltage-type input, and matching to 50 Ω at the outputs is not needed. The most meaningful gain parameter is then the (unloaded) voltage gain. To convert S_{ds21} into voltage gain, 6 dB needs to be added to account for the voltage-halving at the matched output, and an additional 3 dB to take the conversion from 50 Ω input to 100 Ω output into account. Thus, the voltage gain is within 15.1 dB ± 0.5 dB from 100 MHz up to 2.5 GHz. The 3 dB bandwidth is 5.2 GHz.

The π-network formed by an external capacitor (600 fF), the input bondwire inductance (~1 nH) and the input capacitance of the circuit gives a broad input match. Figure 4.9 shows that S_{11} is below -10 dB up to 6.2 GHz. The influence of the ground inductance is included in this measurement, as a Ground-Signal-Ground configuration has been used to bond the input. The common and differential output to single-ended input isolations (S_{sc12} and S_{sd12}, not shown) are better than -30 dB up to 10 GHz.

4.6.2 Noise figure

Figure 4.10 shows that the measured Noise Figure (NF) is below 3.5 dB from 0.2 to 5.2 GHz and below 4 dB from 0.1 to 6 GHz. Another advantageous property of the Noise Canceling technique is that the power and noise matching can be obtained simultaneously [40]. Indeed, the simulated NF equals the simulated NF_{min} of the complete LNA over a large bandwidth and only starts to deviate at higher frequencies due to the increasing impedance mismatch at the input. The increase of NF_{min} at low frequencies is due to $1/f$-noise, the increase at high frequencies is due to the drop in gain.

4.6.3 Gain and phase imbalance

The balun performance was characterized on 20 samples at nominal bias conditions, equal to the simulation conditions. These measurements were performed using wafer-probing. The gain and phase imbalance measurements are shown in Figure 4.11 and 4.12.

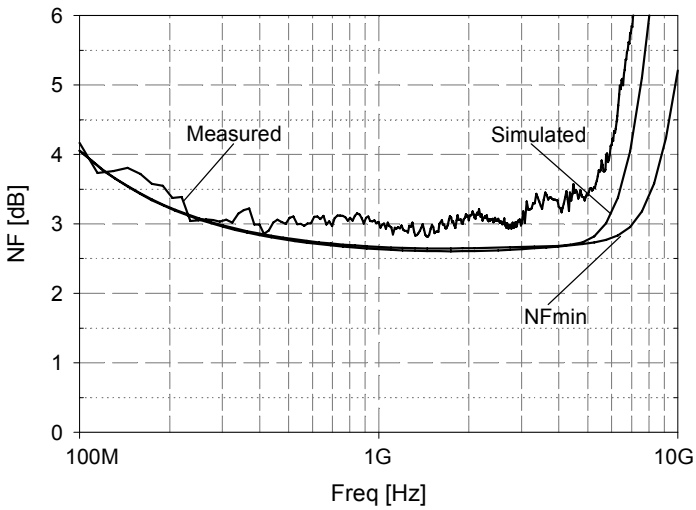

Figure 4.10: Measured Noise Figure, simulated NF and NF_{min} of the complete LNA.

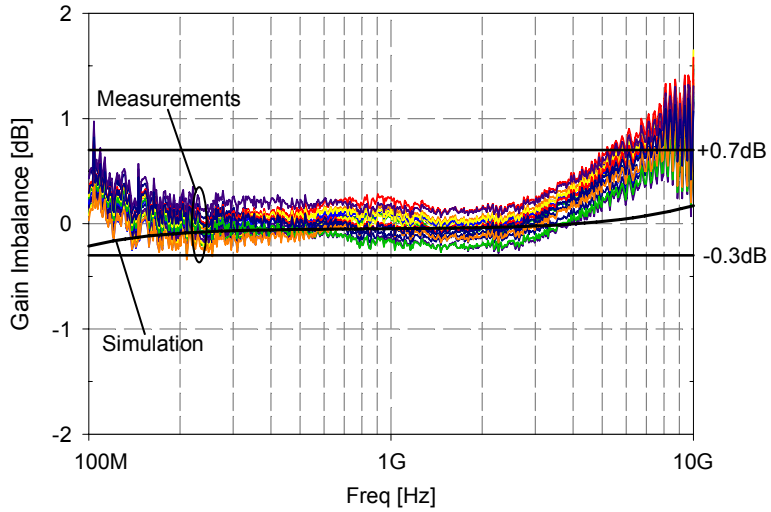

Figure 4.11: Gain imbalance, simulated and measured (20 samples).

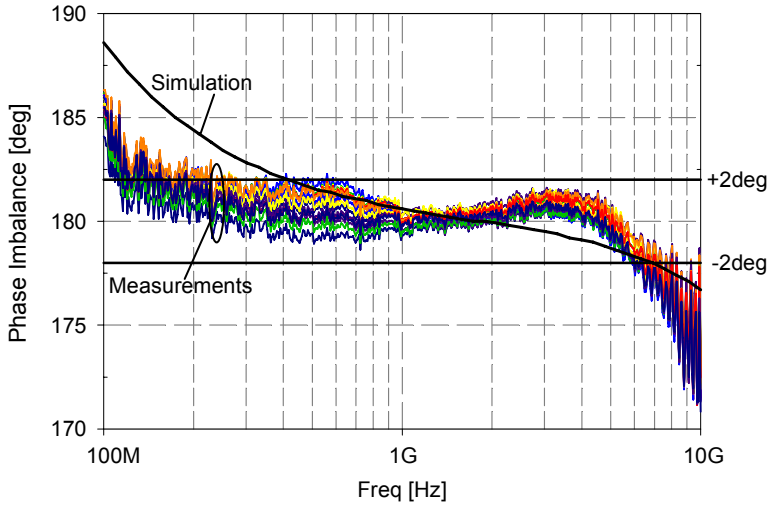

Figure 4.12: Phase imbalance, simulated and measured (20 samples).

The gain imbalance is within +0.7 to -0.3 dB from 100 MHz to 5.2GHz and even within ±0.3 dB in the band 180 MHz – 3.5 GHz. The phase imbalance remains within ±2 degrees from 250 MHz to 6 GHz. The somewhat larger spread in phase difference in the 300 – 800 MHz range is caused by a resonance-effect in the output cables and non-optimal probe contacting. If desired, fine tuning of the balun functionality is possible, e.g. via the bias of the CS or GS stage or via the bulk of the CG transistor.

4.6.4 Linearity

Figure 4.13 shows the 2nd order and 3rd order intercept points versus the frequency of one of the intermodulation tones. To determine the IIP2, one fixed 900 MHz tone (e.g. GSM) is used, whereas another input tone is swept in frequency from 100 MHz to 9.1 GHz. For intermodulation frequencies below 900 MHz the difference frequency is taken, for frequencies above 900 MHz the sum frequency is taken as the intermodulation frequency. An IIP2 of more than +20 dBm over the full 100 MHz – 10 GHz range is achieved. This shows that using the combination of distortion canceling of the CG and the optimum bias for the CS around the gain maximum (see section 4.4), gives low overall 2nd order distortion.

The spread of IIP2 was measured on 20 samples, while keeping the biasing fixed. The worst-case was found to be +18 dBm while other samples showed an IIP2 as high as +34 dBm. To improve this IIP2 value further, and guarantee it over temperature and process spread, it is beneficial to apply calibration techniques, as is more and more done in mixers [56-57]. An effective approach is for instance to use V_{biasCG} to tune the gain of the CS-stage, while using the bulk of the CG-stage to equalize the gain of the CG- and CS-stage. Simulations show a gain error < 0.1 dB for all process-corners and a temperature range of -40 to +100 °C, with a worst case IIP2 = +23 dBm for fast N, fast P at -40 °C and a best case IIP2 = +33 dBm for nominal process at -40 °C (nominal case IIP2 = +27 dBm at 27 °C).

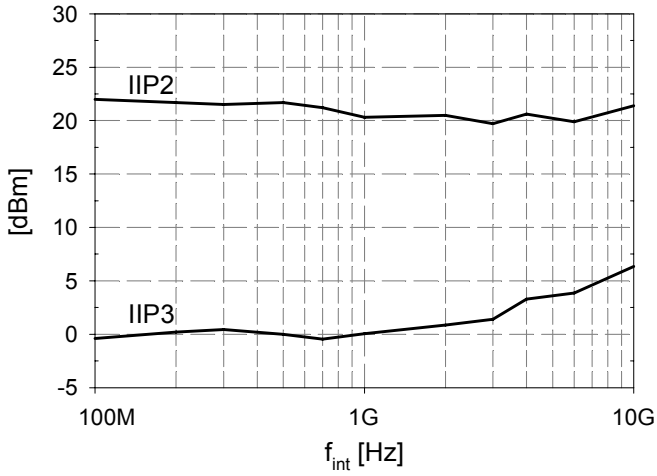

Figure 4.13: IIP2 and IIP3 versus intermodulation frequency (f_{int}).

The IIP3 is determined using two closely spaced tones and is around 0 dBm. The increase in IIP3 with frequency can be explained by the increasing impedance mismatch at the input. The capacitance at the input of the chip input shunts the signal to ground at higher frequencies. Consequently, for the same input power there is less voltage swing on the input-transistors at higher frequencies than in the lower frequency range. This results in less distortion and an increased IIP3. Overall, the results show that capacitive effects in the Balun-LNA play only a minor role over most of the bandwidth.

4.6.5 Benchmarking to other designs

Table 4-I shows a comparison of the balun-LNA to three other wideband CMOS active baluns [14, 20, 43], two passive baluns implemented in CMOS [58] and GaAs [59] and two wideband inductorless single-ended LNAs [40] and [60]. The proposed balun-LNA is more wideband than the passive integrated baluns [58-59] while showing smaller gain and phase imbalances. The LNA performance of the implemented circuit is competitive to non-balun LNAs [40] and [60]. The circuit is integrated in a digital baseline 65nm process using baseline transistors and a 1.2V supply voltage. Still, at this low supply voltage, it achieves high linearity and the active area is small, as no integrated inductors are required. In contrast to [20] the balun-LNA presented in this work simultaneously achieves impedance matching, noise canceling and a well balanced output.

TABLE 4-I
COMPARISON OF BALUN-LNAS, PASSIVE BALUNS AND SINGLE-ENDED LNAS.

Param.	[20] JSSC 2006	[43] CICC 2006	[14] RFIC 2005	[58] MTT-S 2005	[59] MTT-S 2005	[40] JSSC 2004	[60] ISSCC 2006	This Work
Freq. Band [GHz]	0.8 – 6.0	0.9 – 5.0	2.7 – 4.5	0.8 – 2.5	1.5 – 3.5	0.2 – 2.0	0.5 – 8.2	0.2 – 5.2
NF [dB]	< 3.5	< 3.5	< 5	< 4 1)	<1 1)	< 2.4	< 2.6	< 3.5
Gain A_V [dB]	18 – 20	18 – 19	18 – 19.6	S_{ds21} ≈ -4	S_{ds21} ≈ -1	10 – 14	22 – 25	13 – 15.6
IIP2 [dBm]	?	+4 (sim)	?	High	High	+12	?	> +20
IIP3 [dBm]	> -3.5	+1 (sim)	-8	High	High	0	-4 / -16	> 0
Power (core) [mW]	12.5	12	16.2 (12.6)	0 2)	0 2)	35	42	21 (14)
Proc. 3)	90nm	0.13µm	90nm	0.18µm	GaAs	0.25µm	90nm	65nm
V_{supply}	2.5V	1.8V	1.2V	N/A2)	N/A2)	2.5V	2.7V	1.2V
# coils	2	4	1	2	6	0	0	0
Area [mm²]	?	~0.4	0.2	0.073	0.42	0.075	0.025	0.009
Balun?	YES	YES	YES	YES	YES	NO	NO	YES
Gain imbal. [dB]	> 6 5)	?	?	< 0.4	< 1.3	N/A	N/A	< 0.7 < 0.3 4)
Phase imbal. [deg]	?	?	?	< 3.2	< 4	N/A	N/A	< 2

1) Insertion Loss 2) Passive balun 3) CMOS unless specified differently
4) For 180 MHz – 3.5 GHz 5) Derived from component values in schematic

4.7 Conclusions

In this paper we analyzed the performance of a parallel Common Gate (CG) and Common Source (CS) stage for operation as a wideband balun-LNA. We showed that it is possible to achieve simultaneous output balancing, noise canceling and distortion canceling. This requires admittance scaling of the CS-stage with respect to the CG-stage. Compared to a traditional balun design with equally sized CG and CS devices this circuit achieves better noise. Compared to equal load impedance designs, output balancing is achieved and a lower noise figure can be achieved. Moreover, we show that very good linearity can be achieved if the CS-stage has good linearity. In particular, it is shown that an interesting optimum IIP2 point exists in which the $v_{gs} \cdot v_{ds}$-cross-term cancels the traditionally dominant square-law term. Table 4-I shows that this leads to a balun-LNA with very competitive performance in terms of output balancing, noise figure and linearity, while using standard 65nm transistors at the standard 1.2V supply voltage.

Chapter 5

The BLIXER: a compact wideband down-converter topology

This chapter was published in the IEEE Journal of Solid-State Circuits of December 2008 [18]. The publication was invited in the special issue on the 2008 International Solid-State Circuits Conference (ISSCC) based on a publication [17] at this conference.

5.1 Introduction

Wideband radio receivers have recently drawn significant research interest, e.g. for emerging Software-Defined Radio (SDR) architectures and Ultra Wide Band (UWB) Communication standards [20, 61-62]. Such applications ask for radio receivers covering the frequency range from a few hundred MHz up to about 6 GHz (SDR) or even 10 GHz (UWB). Co-operability with other communication devices (e.g. cellular, WLAN) operating in the same spectrum is mandatory, setting especially stringent demands on the wideband linearity of such a receiver. A single-ended RF-input avoids the use of an external broadband balun and its accompanying losses. Compared to a differential input it also requires less switches to connect the RF input to different RF filters and/or antenna networks [62].

Recently some wideband Balun-LNAs with high linearity have been proposed offering a wideband input match, gain and single-ended to differential conversion [15-16]. Active mixers have a capacitive input impedance, i.e. the gate of a transistor. When a passive mixer is used, a

voltage buffer or transconductance stage is often required between the LNA output and the input of the mixer(s). Also this intermediate stage between LNA and mixer loads the LNA capacitively. Due to this capacitance load, it is challenging to realize high LNA gain over a large bandwidth. Inductive peaking has been used to still achieve 6 GHz bandwidth [20, 43], however we would like to avoid the use of area consuming on-chip inductors in expensive nanometer scale CMOS processes. Moreover, the requirements on linearity in the input stage of a mixer will be higher than for the LNA, because of the voltage gain of the LNA. As the input signal of the mixer is still at a high frequency it is challenging to obtain high linearity there. For instance, negative feedback techniques are not very effective because loop gain is limited at GHz frequencies.

This paper proposes a solution to the above described problems via a so called "BLIXER" topology. The topology actually comprises an active balun, LNA and mixer in a single circuit. Without bandwidth extension inductors, it still easily achieves more than 7 GHz bandwidth in 65nm CMOS by merging a current commutating I/Q-mixer with a noise canceling Balun-LNA [17]. In this paper we explain the operation of the topology in detail and analyze its gain and noise behavior. Also we compare it to alternative topologies to illustrate its competitive performance.

The paper is structured as follows: section 5.2 shortly reviews recently proposed Balun-LNAs to show why it is challenging to simultaneously achieve high gain and large bandwidth. Then we introduce the BLIXER topology in section 5.3 and show how it can simultaneously achieve high gain and large RF bandwidth. In section 5.4 we analyze the gain and noise figure of the BLIXER in terms of component design parameters. Section 5.5 discusses the circuit implementation and measurement results, while the conclusions are drawn in section 5.6.

5.2 Balun-LNA gain and bandwidth limitation

5.2.1 Balun-LNA topology

Figure 5.1 shows a Balun-LNA consisting of a parallel operating Common Gate (CG) and Common Source (CS) stage. Both stages are cascoded to allow for realizing a high voltage gain via resistor R_{CG} and R_{CS}. The CG-stage realizes wideband input impedance matching and gain, while the CS-stage realizes an anti-phase output signal. The circuit can simultaneously achieve noise canceling, distortion canceling and output balancing as discussed in detail in [16]. In a CG-stage only, the noise of the CG-transistor would be dominant when the input impedance is matched to R_S ($g_{mCG} = 1/R_S$). However, using a properly designed CS-stage this noise (i_n in Figure 5.1) can be canceled. The noise current (i_n) generates a noise voltage on the source resistor ($v_{n,in}$) and a larger voltage in anti-phase across R_{CG} ($v_{n,CG}$). The input noise voltage ($v_{n,in}$) is amplified by the CS-stage to $v_{n,CS}$, which is in-phase and fully correlated with $v_{n,CG}$. For equal CG- and CS-stage gain, the *noise due to the CG-transistor is fully canceled* at the differential output, while the *signal contributions* to the output signal *add up* to create a balanced output.

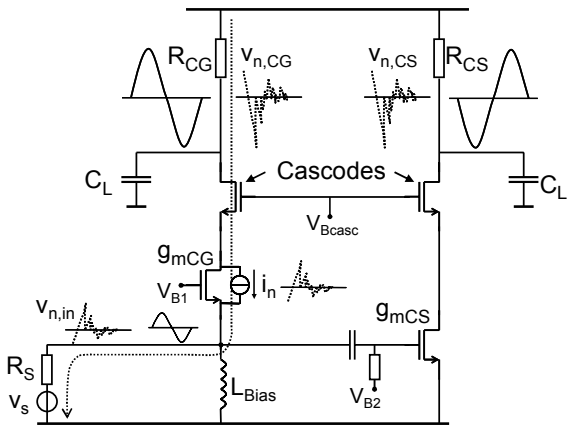

Figure 5.1: Balun-LNA of [16] with cascodes added. Signal v_s is amplified and converted to a balanced RF-output signal, while the noise of the impedance-matching CG-transistor is canceled.

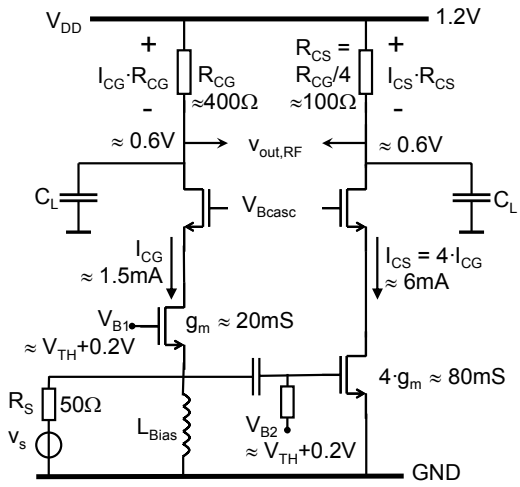

Figure 5.2: Practical Balun-LNA design for *n*=4 illustrating typical component dimensioning and biasing in a 65nm CMOS technology.

This noise canceling technique was proposed in [39-40], while different circuit topologies were generated and compared in [41]. The parallel CS-CG topology (or Balun-LNA) was found to be one of the best performing topologies (topology 'e)' in Fig. 4.22 and 4.23 of [41][1]). It cancels the noise of the CG-transistor in order to obtain a NF close to or lower than 3dB [14-15, 20, 40, 43, 63-64]. To achieve this low NF, the impedance of the CS-stage needs to be scaled down *n* times with respect to the CG stage, where *n* is typically in the order of 4 (see Figure 5.2).

The CG-stage is biased using an external inductor (L_{bias}) to obtain low-noise operation and save valuable voltage headroom. Depending on the application this inductor can either be very large (RF-choke) for wideband operation, or smaller and well-defined to tune to a dedicated band and realize RF pre-filtering. Especially for software

[1] Reprinted in this thesis as Figure 2.6 and 2.7, while the topologies can be found in Figure 2.5.

defined radio transceivers this is a realistic approach, as some RF-pre-filtering is commonly needed to make the linearity requirements of a CMOS transceiver feasible [13]. Using an external inductor at the input of a CMOS chip allows for realizing external re-configurability and generally the quality factor of the off-chip inductors is higher than on-chip realizations.

5.2.2 Achievable gain and bandwidth

The voltage gain of transistors in modern CMOS processes is low. Cascoding is an effective method to increase the voltage gain. The output resistance of the transconductor (input transistor plus cascode) is increased, so that increasing R_{CG} and R_{CS} in Figure 5.1 still improves the voltage gain. Next to this, the cascodes lower the effective input capacitance, as the 'Miller' effect is reduced (most important for the CS-transistor, as it is *n*-times wider than the CG-transistor). This helps to improve the bandwidth over which good input impedance matching is achieved.

Let us now consider the gain and bandwidth of the Balun-LNA, neglecting the effect of body effect for simplicity. In Figure 5.2 a typical design in a 65nm CMOS technology is shown. The transconductance of the CG-transistor is 20 mS to realize impedance matching to a 50 Ω source. This requires about 1.5 mA of biasing current for a transistor with W/L = 90 µm / 0.06 µm at a moderate overdrive voltage of $V_{GT} \approx 0.2$ V. We design the voltage drop across the load resistor to be 0.6 V, half of the 1.2 V supply voltage. This leaves 0.6 V for the sum of V_{DS}'s of the input and cascode transistor, which is sufficient to keep each MOS transistor in saturation ($V_{DS} > V_{GT}$). With 1.5 mA bias current in the CG-stage and 0.6 V headroom, the CG load resistor (R_{CG}) becomes 400 Ω. If we use the same components and biasing in the CS-stage, and neglect the body effect, than DC-bias and modulus of the gain of the stages are equal. Since the CG noise is canceled, the CS noise dominates in the LNA. To achieve acceptable noise, the impedance level in the CS-stage is assumed to be scaled down by 4 times (80 mS and 100 Ω). This does not affect the DC-voltages and voltage gain. With $g_{m,CG}$ = 20 mS and R_{CG} = 400 Ω, the voltage gain of the CG-stage is:

$$A_{V,CG} = g_{mCG} \cdot R_{CG} = 20 \cdot 10^{-3} \cdot 400 = 8 \tag{5–1}$$

As the gain of the CS-stage is equal but with opposite sign, the total voltage gain of the CG-CS LNA from single-ended input to differential output is 2 times higher:

$$A_{V,CG-CS} = 2 \cdot A_{V,CG} = 16 \Leftrightarrow 24\ dB \tag{5–2}$$

A high voltage gain can thus be obtained by using this parallel connection of a CG- and a CS-stage. However, the bandwidth associated with this high gain is limited due to the dominant pole at the output of the CG-stage. For a 3 dB-bandwidth of 10 GHz, the loading capacitance (C_L) is most critical at the CG-side and should be smaller than:

$$C_L < \frac{1}{2\pi \cdot R_{CG} \cdot f_{-3dB}} = \frac{1}{2\pi \cdot 400 \cdot 10 \cdot 10^9} = 40\,fF \tag{5–3}$$

The load capacitance is the sum of the input capacitance of the next stage (input stage of the mixer) and the capacitance of the cascode transistor. For a cascode transistor with W/L = 90/0.06 µm (same size as the CG-transistor), the capacitance of the only the cascode is already close to the maximal allowed capacitance:

$$C_{Casc} \approx C_{GDO} + C_{JDB} = 15f + 22f = 37\,fF \tag{5–4}$$

where the two dominant capacitances seen at the drain of the cascode are the gate-drain overlap capacitance (C_{GDO}) and the drain-bulk junction capacitance (C_{JDB}). This means that no (capacitive) load can be driven when a 3 dB-bandwidth in the order of 10 GHz is required. This clearly shows that there is a bandwidth problem at the load of the CG-side for high enough voltage gain. As one of the goals in this design was to avoid the use of on-chip inductors, no inductive peaking techniques [20, 43] will be used to broaden the bandwidth. The BLIXER topology we propose in the next section achieves this large bandwidth without requiring on-chip inductors.

5.3 The BLIXER Topology

5.3.1 The basic BLIXER topology

In Figure 5.3 the principle of the BLIXER topology is shown. Compared to the Balun-LNA of Figure 5.1, the same CG- and CS- transistors are used while the cascode transistors are now part of a current commutating mixer. Instead of one, both the CG- and the CS-side have now two cascode (or mixer) transistors, which are periodically switched on and off, with frequency f_{LO}. The current from the CG- and CS-transistor can always flow towards the loads, as at any moment in time one of its mixer (cascode) transistors is active, i.e. the LO signal has 50% duty-cycle. At the drains of the mixer the signal of interest is down converted to an "intermediate frequency" (IF) which is much lower than the RF frequency. In the BLIXER topology, the capacitance at the loads sets the *IF-bandwidth*, instead of the *RF*-bandwidth in case of the Balun-LNA. As the IF-bandwidth is much lower than the RF-bandwidth, the capacitance at the loads can be much higher. Furthermore, the capacitive load of the next stage can be absorbed into the capacitance of the IF-filter. The bandwidth problem at the

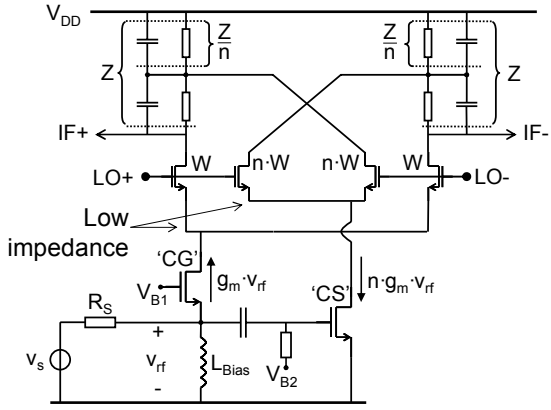

Figure 5.3: Basic BLIXER topology consisting of the Balun-LNA core of Figure 5.1 with doubled cascode transistors driven by an LO implementing down-conversion mixing to IF.

load of the CG-stage, described in the previous section, is thus solved without requiring inductors for bandwidth extension.

There are only three RF-signal nodes in the BLIXER topology; the input and the drains of the CG- and CS-transistor. This means that in the complete down-converter there are only three nodes that can limit the RF-bandwidth. For impedance matching, the real part of the input impedance of the circuit equals R_S (50 Ω). When the real part of the impedances at the two drains nodes is low (indicated in Figure 5.3), the bandwidth at these nodes is large. For switch transistors equal to the cascode transistors in Figure 5.2, the real parts at the drains of the CG- and CS-transistors are 50 Ω and 12.5 Ω respectively ($=1/g_m$ of mixer transistors). Thus all RF node impedances are in the order of 50 Ω or lower, allowing for large bandwidth.

The CG- and CS-transistors can be considered as a transconductor converting v_{rf} to currents $g_m \cdot v_{rf}$ and $n \cdot g_m \cdot v_{rf}$ (see Figure 5.3). These currents are largely conveyed to the IF output via the switched cascode transistors, provided the real input impedance of these transistor is lower than the parasitic capacitance to ground. Only modeling gate-source capacitances, the RF-bandwidth limitation due to the switched cascode transistors will be close to $f_T = g_{m,switch} / C_{GS,switch}$, which is typically an order of magnitude higher than for the balun-LNA with a voltage gain in the order of 20 dB.

5.3.2 Noise canceling at IF instead of at RF

Now consider the real part of the load impedance which consists of 4 resistors instead of 2 in the Balun-LNA. This is done to maintain the noise canceling conditions in both LO-switch positions. In Figure 5.4 the active part of the circuit is shown when LO+ is high. As in Figure 5.1, the CG-side has Z as load, while the load in the n times scaled CS-side is Z/n. The IF-output voltage is sensed at the combined CG- and CS-load, where the lower capacitance of the current-less branch effectively works as level shifter. As the impedance of the CS side is n times lower than for the CG-side, it has a low noise contribution and still the gain of the CG- and the CS-sides is equal. As the gain of both sides is equal, the noise of the CG-transistor is canceled in the same way as in the Balun-LNA of Figure 5.1.

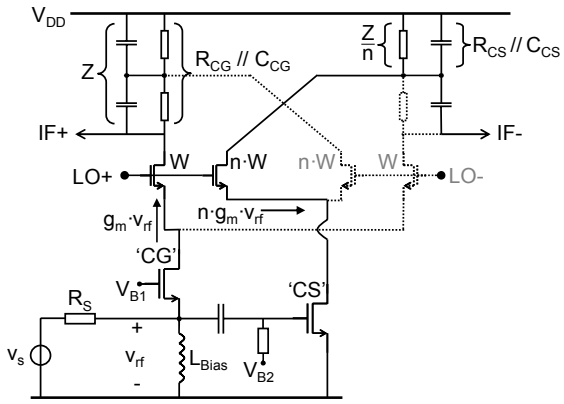

Figure 5.4: Equivalent circuit for the BLIXER during when LO+ side is active. As in Figure 5.1, the current of the CG-stage flows into its load impedance R_{CG} ($//C_{CG}$), and the CS current flows into R_{CS} ($//C_{CS}$), which impedance is n times smaller.

Note that in the BLIXER topology the noise canceling takes place after the frequency (down) conversion i.e. at IF. The noise canceling down-converter in [65] also has this property. However, it is much less power efficient as *cascaded* stages instead of cas*co*ding (i.e. stacking of transistors with current re-use) was used, while also high overdrive voltages were used to push the bandwidth.

5.3.3 The I/Q-BLIXER topology

Quadrature outputs are required in order to implement a low- or zero-IF receiver. It is possible to create quadrature outputs starting with signal currents i and $-i$ from a differential pair, by connecting two switching pairs to each current, and using a sine and cosine wave to drive the two pairs [66-67]. In principle this is also possible with the asymmetrical Balun-LNA currents i and $-4i$, provided that the switch transistors and load network are scaled as shown in Figure 5.5.

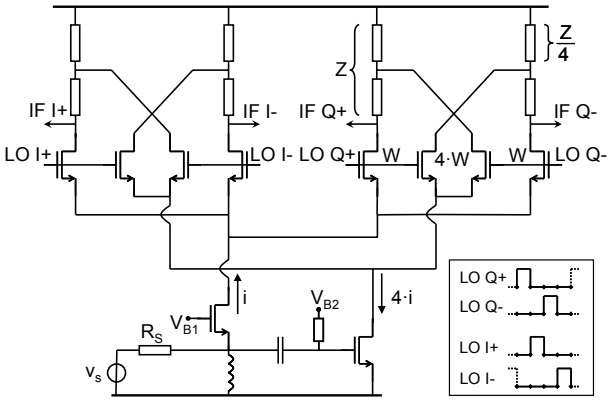

Figure 5.5: I/Q-BLIXER driven by LO waveforms with 25% duty cycle, which allows for sharing currents *i* and *4·i* by an I- and Q-mixer.

We will refer to this circuit as the "I/Q-BLIXER". Simulations show that it is possible to use sine and cosine LO-signals with in I/Q Blixer, however this seems mainly attractive for narrowband receivers like in [66-67]. For narrowband receivers, the required sine and cosines can be generated via a quadrature VCO with relatively small tuning range. For multi-standard receivers or software defined radio we want much wider tuning range and digital frequency synthesis methods exploiting Moore law are preferred [68]. However, using two square waves with 50% duty cycle with a relative delay of 1/4 period gives 25% overlap between LO-I and LO-Q pulses. Using a 25% duty-cycle, this overlap can be avoided and it is possible to "isolate" the I- and Q-current-path in time. Hence, the full g_m of the input devices is available to either the I- or Q-output of the circuit which is beneficial for the conversion gain. Furthermore, we will show in the next section that, without compromising the voltage headroom, it is possible to double the value of the IF-load resistors to increase the gain.

5.3.4 Conversion gain and voltage drop load resistors

The voltage conversion gain from single-ended input to differential output of the BLIXER topology (Figure 5.3) can be calculated as:

$$\begin{aligned} G_{Blixer} &= \frac{2}{\pi} \cdot \left(g_{mCG} \cdot R_{CG} + g_{mCS} \cdot R_{CS} \right) \cdot 2 \cdot \frac{1}{2} \\ &= \frac{2}{\pi} \cdot \left(g_{mCG} \cdot R_{CG} + g_{mCS} \cdot R_{CS} \right) \end{aligned} \tag{5–5}$$

where, after the 1st equal-sign, the factor $2/\pi$ equals the fundamental Fourier component of a 50% duty-cycle (LO)-signal toggling between 0 and 1. The term between brackets is the combined voltage gain of the CG and CS-side. The factor 2 is to convert from single-ended to differential, and the final factor 1/2 is because only the down converted half of the signal is used, as shown in equation (5–6):

$$\begin{aligned} s(t) &= \cos(\omega_{Signal} t) \cdot \cos(\omega_{LO} t) \\ &= 1/2 \cdot \cos\left((\omega_{Signal} - \omega_{LO}) t \right) \quad \rightarrow \text{down converted} \\ &+ \cancel{1/2 \cdot \cos\left((\omega_{Signal} + \omega_{LO}) t \right)} \quad \rightarrow \text{up converted} \end{aligned} \tag{5–6}$$

Similarly, the voltage gain of the I/Q-BLIXER (Figure 5.5) with 25% duty-cycle LO equals:

$$G_{IQBlixer} = \frac{\sqrt{2}}{\pi} \cdot \left(g_{mCG} \cdot R_{CG} + g_{mCS} \cdot R_{CS} \right) \tag{5–7}$$

where, the factor $\sqrt{2}/\pi$ equals the fundamental Fourier component of a 25% duty-cycle LO-signal. Compared to the BLIXER, the conversion gain of the I/Q-BLIXER is lower due to the lower duty-cycle, assuming the same g_m's and load resistors are used. However, in the I/Q-BLIXER larger load resistors can be used, as shown below.

The average (or DC) voltage drop across the load resistors in the BLIXER is:

$$\overline{V_{Load}} = \frac{1}{2} \left(I_{CG} \cdot R_{CG} + I_{CS} \cdot R_{CS} \right) \tag{5–8}$$

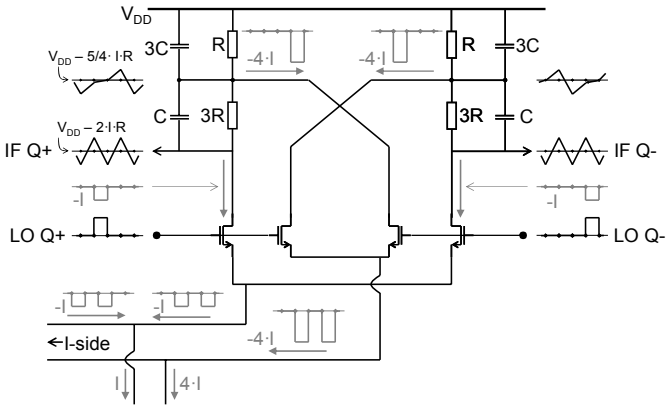

Figure 5.6: Q-side of the I/Q-BLIXER showing the branch currents and node voltages.

This is because with 50% duty-cycle LO, half of the period the CG-transistor bias current (I_{CG}) flows through R_{CG} and in the other half the CS-bias current (I_{CS}) a current flows through R_{CS}.

In the I/Q-BLIXER the DC-voltage drop across the load equals:

$$\overline{V_{Load}} = \frac{1}{4}\left(I_{CG} \cdot R_{CG} + I_{CS} \cdot R_{CS}\right) \qquad (5\text{–}9)$$

as with 25% duty-cycle the CG- and CS-bias current flow only for ¼ of the period through one of the loads (the waveforms are shown in Figure 5.6). The capacitors in the load 'average' these pulses of current and filter out the high-frequency components.

Comparing (5–8) with (5–9) we see that, assuming equal transconductor bias currents (I_{CG} and I_{CS}) and equal voltage drop across the load, we can double the load resistors (R_{CG} and R_{CS}) in the I/Q-BLIXER. This doubling of the load resistors (+6 dB) compensates the gain reduction caused by the lower duty-cycle (-3 dB) and results in 3 dB more conversion gain for the I/Q-BLIXER compared to a 50% duty cycle BLIXER.

A numerical example clarifies this further. Using exactly the same components and biasing as the Balun-LNA of Figure 5.2 for the BLIXER results in the same voltage drop across the load resistors (0.6 V). Using (5–5) the conversion gain equals: G_{Blixer} = 20 dB, which is about 4 dB lower ($2/\pi$) than the gain of the Balun-LNA. In the I/Q-BLIXER we can double the load resistors, i.e. R_{CG} = 800 Ω and R_{CS} = 200 Ω. This results in an I/Q-BLIXER with a gain of $G_{IQBlixer}$ = 23 dB, which is only 1 dB lower than the Balun-LNA, and 3 dB higher than the BLIXER.

5.3.5 Similar topologies in Literature

In [48] a "MICROMIXER" cell with single-ended input and differential output was proposed. It uses a bipolar equivalent of the CG-CS input stage. However the possibility of noise canceling was not recognized nor exploited. Two of these mixer-cells and an additional LNA would be needed for I/Q-operation with acceptable NF.

A merged LNA and I/Q-mixer was published in [66]. However, this design is narrowband, uses 3 on-chip inductors and requires a differential RF-input signal. In contrast, the I/Q-BLIXER topology does not require on-chip inductors, achieves wideband single-to-differential operation and I/Q-mixing in one circuit cell.

In [69], a 'merged CMOS LNA and Mixer exploiting noise cancellation' is proposed, which seems related at first sight ("merged" and "noise cancellation"). However, a closer look shows this combination actually uses a folded mixer with separate bias currents for the LNA and mixer core (no current re-use). Also the used noise canceling is of another type, rendering partial canceling. This circuit has no I/Q outputs, requires a differential input (and external balun) and uses 4 on-chip inductors. Still, the circuit also uses down-conversion via current commutation directly on the output current of a CG input stage, and is in that sense related. We will compare its performance at the end of this chapter (see Table 5-I in section 5.5).

5.3.6 Attractive properties of BLIXER topologies

Apart from the bandwidth advantages, the BLIXER topology has some other advantageous properties with respect to linearity, balancing of the output and power consumption, as discussed below.

Similar as the noise, the distortion generated by the CG-transistor is canceled [15-16, 63] and the load resistors are linear. If the switch transistors are well switched, the mixer transistors convey the output current of the CG-CS stage to the output without much distortion (assuming $1/g_m$ is significantly lower than the somewhat nonlinear output impedance of the CG/CS-transistors). This means that the only remaining source of non-linearity in the BLIXER is the V-to-I conversion of the CS-transistor. In a traditional cascade of voltage-gain LNA and active mixer, the mixer input transistors experience almost an order of magnitude more voltage swing than the transistors at the RF input, hence the mixer transistors often limit the overall linearity. As the CS-transistor of the BLIXER directly senses the RF-input voltage *without pre-amplification*, relatively high linearity can easily be obtained.

Compared to the Balun-LNA of Figure 5.1, the BLIXER also improves on the quality of the balance of the output signal. This is because the output load network is completely symmetrical in the BLIXER, instead of the Z and Z/n in the Balun-LNA. Moreover, *both the CG- and CS-stage* contribute to *both* of the output signals (each half of the time). Even if the ratio between the $g_{m,CG}$ and $g_{m,CS}$ is not exactly equal to the ratio of the *CS*- and *CG*-load impedances (*1:n*), still the gain balancing at the IF-output is unaffected. Such a mismatch does make the noise canceling less perfect, but as shown in [39, 41] noise canceling is robust for such errors as ±20% mismatch still only gives 0.1 times the noise of the CG transistor (without canceling).

The power efficiency of the BLIXER is also attractive as the bias-current of the Balun-LNA is re-used to realize the mixer functionality. Especially when the I/Q configuration is used, a complete I/Q down-conveter with high conversion gain is obtained re-using the power of the Balun-LNA. Of course, the LO-drivers do require additional power,

but this power will scale down in future technologies with Moore's law.

5.4 Implementation and simulations

In the following sections we will discuss the actual chip implementation of the I/Q BLIXER in a 65nm CMOS technology and we will evaluate its performance via simulations, comparing the I/Q BLIXER to the Balun-LNA and the basic BLIXER.

5.4.1 Input transconductor implementation

The implementation of the input transconductor is shown in Figure 5.7. As discussed in section 5.3.6 the CS-stage determines the linearity of the circuit. In order to obtain high (3rd-order) linearity the CS-transistor should be biased with a high V_{GT}. However, at a high V_{GT} the g_m/I_D of a transistor is low, which means that a large bias current is required to reach a certain g_m. This reduces the voltage headroom as this bias current has to flow through the loads. Therefore, the CS-stage is implemented using a PMOS and a NMOS transistor. Both the NMOS and PMOS can be biased at a high V_{GT} for high 3rd order linearity, whereas also the 2nd order distortion can be low in this inverter-type of circuit. The effective g_m of this inverter based CS-stage is designed to be about 4 times higher than the effective g_m of the CG-transistor. Also the DC-output current the CS-stage inverter ($I_{CS} = I_{NMOS} - I_{PMOS}$) is designed to be approximately 4 times higher than the bias current of the CG-transistor. Besides the high linearity, another advantage of the inverter-type CS is that the PMOS transistor can be DC-coupled to the input, which reduces the AC-coupling related signal-loss to the input of the CS-stage.

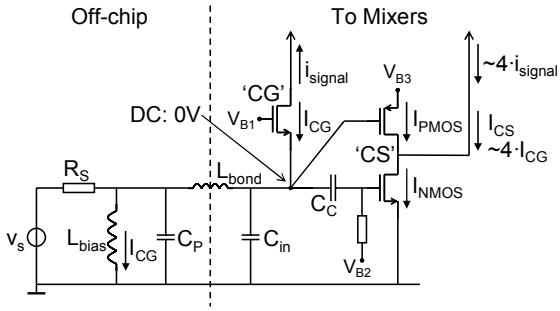

Figure 5.7: Implementation of the input stage. The CS-transistor is split is a PMOS and an NMOS transistor.

The CG-transistor is biased using an inductor which puts the source of the CG-transistor at DC-ground, as indicated in Figure 5.7. Because the biasing of the CG-transistor does not require any DC-voltage drop, the voltage headroom of the CG- and CS-side is equal. A large bias inductor (L_{bias}~40 nH) can be used as it is placed off-chip. This large inductor allows for good matching in the lower frequency range. In the higher frequency range, the parasitic capacitance of the inductor (C_{par}) dominates. Together with the total bondwire inductance and input capacitance (L_{bond} and C_{in}) a broadband-matching π-network is formed, which results in impedance matching up to high frequencies.

5.4.2 Switches and load implementation

The width of the switches switching the CG-current was chosen at 40% of the width of the CG-transistor. The reason for choosing a small(er) width is to reduce the input capacitance of the switches. The area of a transistor determines its *1/f*-noise. In order to lower the *1/f*-noise contribution of the switch transistors, their area was increased by setting the length to 100 nm, instead of using minimum length (65 nm) devices. As overlap and junction capacitances dominate the capacitance of transistors with small length, increasing the length increases the input capacitance of the switches only slightly. The CS-switches are 4 times wider than the CG-switches.

The impedance ratio of the CG- and CS-part of the load was designed equal to the ratio of effective CS- and CG- transconductance, which is nominally slightly lower than 4. The bandwidth of both parts of the loads was designed in the order of 300 MHz, enough to handle UWB signals in a zero-IF architecture.

5.4.3 Conversion gain and noise figure simulations

In this section we will evaluate the performance of the BLIXER and the I/Q-BLIXER to each other and compared to a stand-alone Balun-LNA. The aim of this comparison is to show that the BLIXERs can have more bandwidth, at practical values for the gain and noise figure. In order to make a fair comparison, all three circuits use the input stage described in section 5.4.1, and the dimensions of the (switched or biased) cascode transistors are equal. As discussed in section 5.3.4, the load impedance of the BLIXER and the Balun-LNA needs to be half the load impedance of the I/Q-BLIXER, in order to keep the average voltage drop across the loads equal in all three cases. The loads in the Balun-LNA and BLIXER are halved by placing two I/Q-BLIXER loads in parallel. The switches of the BLIXER and I/Q- BLIXER are driven with ideal 50% and 25% duty-cycle LO-signals respectively (rise- and fall-time 1% of the LO-period).

Figure 5.8 shows the voltage conversion gain of the BLIXERs as a function of the input signal frequency for an IF of 50MHz. Also the voltage gain versus signal frequency of the Balun-LNA, loaded with 100fF on both outputs, is shown.

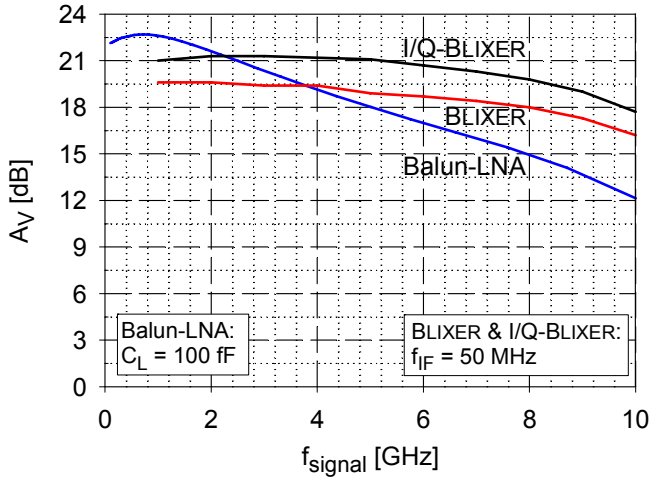

Figure 5.8: Gain of the Balun-LNA, basic BLIXER (50% LO duty-cycle) and I/Q-BLIXER (25% LO duty-cycle). Note that the BLIXERS have much larger bandwidth (9.5GHz).

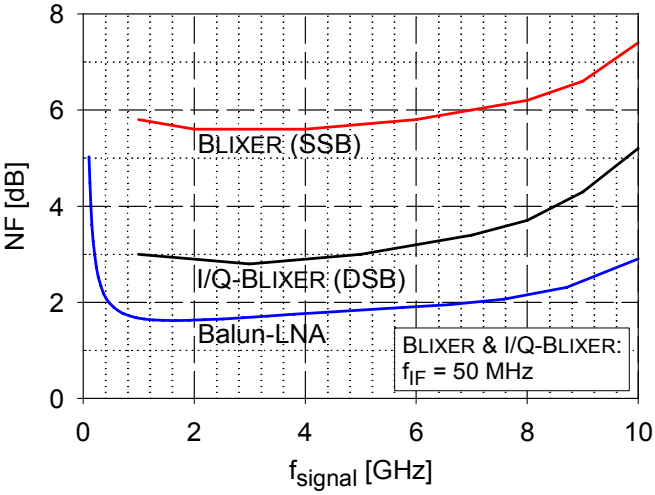

Figure 5.9: Comparison of the Noise Figure of the Balun-LNA, basic BLIXER and I/Q-BLIXER.

Clearly, the bandwidth of the BLIXERs is much larger (~9.5GHz) than the bandwidth of the Balun-LNA (~3.5 GHz). As expected, the (low frequency) conversion gain of the I/Q-BLIXER is about 1 dB lower than the gain of the Balun-LNA.

Figure 5.9 shows the Noise Figures of the three topologies. The *Single* Side Band (SSB) Noise Figure of the BLIXER is ~4 dB higher than the NF of the Balun-LNA. This can be expected based on the conversion-gain of the mixing action ($2/\pi$ or -4 dB). In contrast to the BLIXER, the I/Q-BLIXER has I- and Q-outputs which can be combined to reject the noise of the image band. Therefore, the relevant measure of noise figure for the I/Q-BLIXER is the double side band (DSB) noise figure. Figure 5.9 shows that compared to the stand-alone Balun-LNA, the NF of the I/Q-BLIXER increases with only 1–2 dB.

5.4.4 Effects of non-ideal LO-signals

For higher LO-frequencies it becomes increasingly challenging to generate a 25% duty-cycle LO-signal with sufficiently low rise- and fall-times. Simulations on the I/Q-BLIXER are performed to investigate the effects of finite rise- and fall-times. An ideal voltage source generating a 25% duty-cycle LO-signal with 10% rise and fall-time is supplied to a cascade of two inverters, for each of the 4 LO phases. The inverters used for this simulation are equal to the inverters used in the final stage of the LO-driver in the complete I/Q-BLIXER realization. The size of second inverter is twice the size of the first inverter, and is designed to drive the LO-switches. The inverters limit the rise and fall time to about 25–30 ps, which causes narrower pulses and lowers pulse-amplitude for higher LO-frequencies.

Figure 5.10 shows that for higher LO-frequencies, mainly the NF at low IF-frequencies (2 MHz) is affected. The increase in NF at low IF-frequencies is due to an increased sensitivity to *1/f*-noise of the LO-switches and the LO-driver (inverter) transistors. The reduction of conversion gain compared to the case with ideal LO-drive is smaller than 1 dB (not shown as this is only a minor effect).

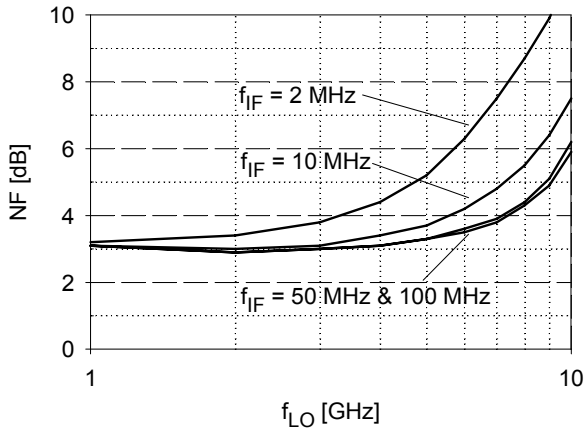

Figure 5.10: Effect of LO-pulse with finite rise and fall time in the I/Q-BLIXER on the NF versus the LO-frequency for different IF-frequencies.

5.5 IC implementation and measurements

Figure 5.11 shows an overview of the I/Q-BLIXER test chip. The RF-input is single-ended while the IF I- and Q-outputs are differential. The single-ended external oscillator signal is converted to differential on-chip and subsequently divided by 2 to generate in-phase (I) and quadrature (Q) LO-signals. The output of the divide-by-2 is amplified to rail-to-rail swing to obtain a 50% duty-cycle LO signal. The required 25% duty-cycle is generated using an 'AND'-operation on the I- and Q-signals. The I/Q-BLIXER core is implemented as described in section 5.4.1 and 5.4.2. For measurement purposes the differential IF-outputs of the I/Q-BLIXER are buffered to 50 Ω, using 4 source followers.

The circuit was fabricated in a baseline 65nm LP CMOS technology and a standard 1.2V supply was used. The die photo and a detail of the PCB are shown in Figure 5.12. The I/Q-BLIXER core measures less than 0.01mm^2. The measurements were performed on packaged, PCB-mounted samples.

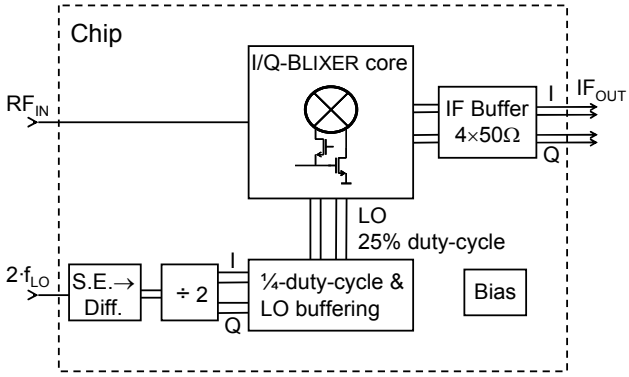

Figure 5.11: Overview of the test chip. The LO is derived from an external clock via a single-to-different converter and divide-by-2 to generate quadrature phases.

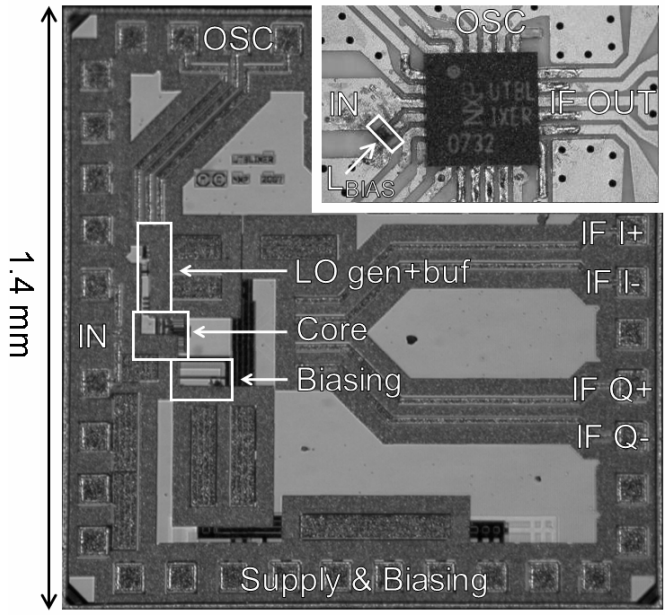

Figure 5.12: Chip micrograph and PCB detail (top right) showing packaged sample.

The measured voltage conversion gain is 19 dB with and the IF-bandwidth is 400 MHz, as shown in Figure 5.13. The DSB NF of the I/Q-BLIXER at a 3 GHz LO frequency is around 4.5 dB and flat over the IF bandwidth.

The wideband RF performance is shown in Figure 5.14. The gain remains flat within 1 dB up to 7 GHz. From 1 to 6 GHz the NF is below 5 dB, using a fixed IF of 50 MHz. Note that this NF includes the PCB losses. Above 7 GHz the circuit generating the 25% duty-cycle LO-signals fails and the gain and NF could not be determined. The S_{11} is below -10 dB up to 7 GHz.

The wideband linearity was measured using a two tone test. To assess IIP2 and IIP3 without filtering effects, the input tones and the intermodulation products should fall within the flat part of the conversion gain versus frequency curve (Figure 5.14). In a wideband system a high spacing between the two test tones can be used. Two tones at 5.2 GHz and 5.7 GHz, which represents two IEEE 802.11a interferers, gives a 3rd order intermodulation product at 4.7 GHz. Using an LO frequency of 4.6 GHz the measured IIP3 = -3 dBm. The IIP2 equals +20 dBm, using 2.4 GHz (802.11b/g) and 5.7 GHz (802.11a) input tones and an LO of 3.2 GHz. The intermodulation for tones that leak through the mixer was determined using a 5.7 GHz and a 5.8 GHz signal (two 802.11a interferers). The intermodulation product at 100 MHz showed an IIP2 > +40 dBm, regardless of the LO frequency. The LO leakage to the RF input is below -60 dBm for LO-frequencies up to 4 GHz and below -50 dBm up to 7 GHz.

Figure 5.15 shows a breakdown of the power consumption of the different parts of the implemented circuit. The I/Q-BLIXER core consumes 16 mW and the Biasing and IF-Buffering combined consume 13 mW. Note that the IF-buffers are added for measurements purposes and can often be omitted. At an LO-frequency of 500 MHz, the 25% duty-cycle generation and LO-buffering consume only 4 mW. At an LO-frequency of 7 GHz this part consumes 28 mW, which is almost half of the total power consumption. The LO-buffering is based on inverters, which explains the increase in (dynamic) power consumption at higher LO-frequencies.

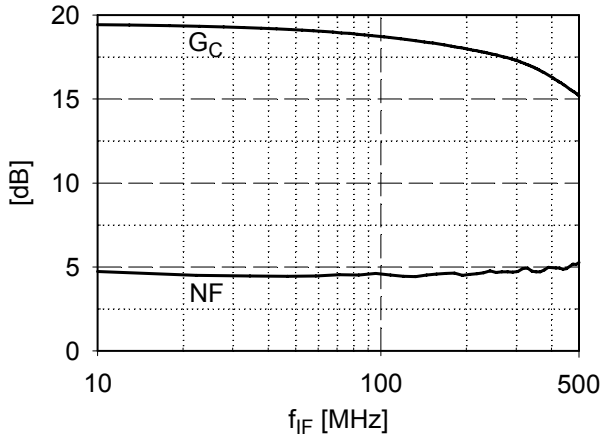

Figure 5.13: Conversion Gain (G_C) and NF for f_{LO} = 3 GHz.

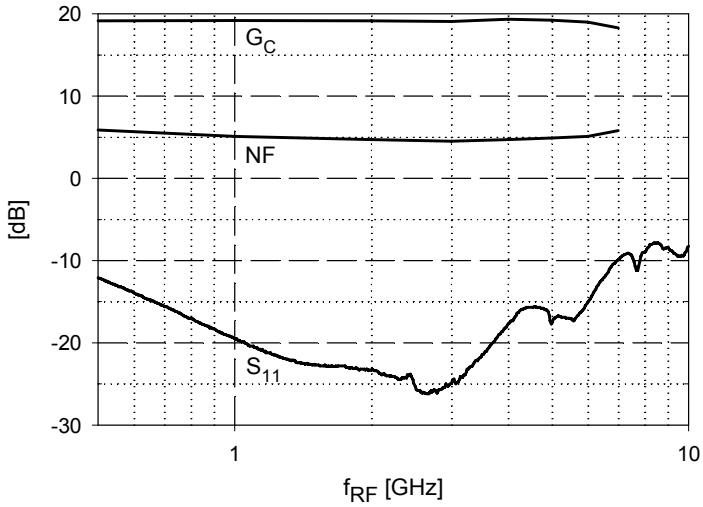

Figure 5.14: Conversion Gain (G_C), NF and S_{11} versus RF input-frequency (f_{IF} = 50 MHz).

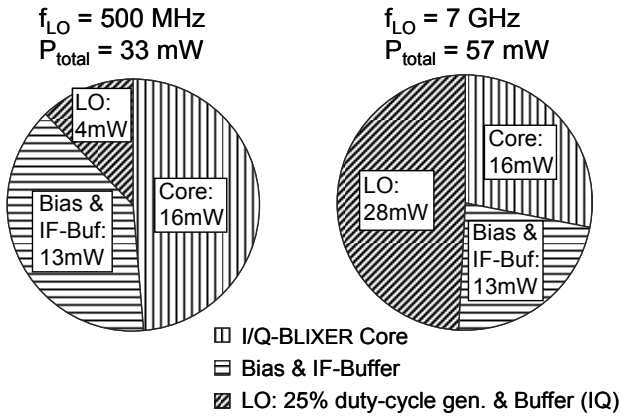

Figure 5.15: I/Q-BLIXER power consumption breakdown for 500 MHz and 7 GHz.

In Table 5-I the measured performance is summarized and compared to other state-of-the-art wideband down-converters. The I/Q-BLIXER achieves the largest signal bandwidth. Note that we specify the -1 dB bandwidth, where others often specify the -3 dB bandwidth. The obtained linearity is the highest among the reference designs. The main reason for the high linearity is that the (RF) linearity is determined by only one transistor (combination), the CS-inverter.

The noise figure is comparable to the other designs; furthermore, the NF is almost flat across the entire band. Note that this NF includes the PCB-losses and that no external balun is needed.

Due to the absence of on-chip inductors, the area is very small. The combined area of the I/Q-BLIXER core and the I/Q-LO Buffers is more than 4.5 times smaller than the smallest reference design.

For low LO-frequencies the power consumption of the LO buffering is much lower than the other designs and for high LO-frequencies it is in the same order. The design of [69] has a lower core (LNA plus Mixer) power consumption. However, in contrast to our design, this design has no quadrature outputs. Compared to the designs with quadrature outputs [20, 61-62], the power consumption of our design is about 2 times lower.

TABLE 5-I
COMPARISON OF STATE-OF-THE-ART WIDEBAND DOWN-CONVERTERS

Parameter	Lee ISSCC '07 [61]	Craninckx ISSCC '07 [62]	Bagheri JSSC '06 [20]	Amer JSSC '07 [69]	This Work
RX Freq. [GHz]	2 – 8	1.8 & 5 – 6	0.8 – 6	0.1 – 3.85	**0.5 – 7**
Gain [dB]	23 incl. IF-Amp	10 – 90 incl. IF-Amp	3 – 36 incl. IF-Amp	20 incl. IF-Amp	18 *excl.* IF-Amp
IIP3 [dB]	-7	-9	3.8	-3.2 [1)]	**-3**
IIP2 @ RF [dB]	+18	?	?	?	**+20**
NF [dB]	4.5	4 – 8	5 – 5.5	8.4 – 11.5 (SSB)	4.5 – 5.5
S_{11} [dB]	< -8	< -9	< -10	< -10	< -10
Area [mm²]					
LNA + IQ-Mixers	0.09	0.6	0.5	0.88 (only I-path)	**< 0.01**
LO Buff. (I & Q)		0.3	?	?	**< 0.01**
Power [mW]					
LNA + IQ-Mixers	38	34 WLAN setting	29 (I & Q?)	9.8 (only I-path)	**16**
LO Buff. (I & Q)	24	17 WLAN setting	?	?	4 – 28
CMOS Technology	65nm	0.13µm	90nm	90nm	65nm
VDD	1.2V	1.2V	2.5V	1.2V	1.2V

[1)] Estimated using $P_{IIP3} = P_{1dB\,CP} + 9.6$ dB [9]
[2)] Estimated from chip micrographs

5.6 Conclusions

This paper proposes the "BLIXER" topology which stacks a current-commutating mixer on top of a Noise Canceling Balun-LNA. The proposed topology has several attractive properties. It achieves a high and flat gain over a large bandwidth without inductors for bandwidth extension. This is because the BLIXER directly converts the currents of the Balun-LNA core to IF via current-commutating mixers, of which the (real part of) the input impedance is low. Creating voltage gain is shifted from RF to baseband (IF), where capacitive loading is no problem.

By using an I/Q mixer with 25% duty-cycle LO-waveform, the output IF-currents have also have a reduced duty-cycle, resulting in smaller DC-voltage drops after IF filtering. This allows for a 2 times increase of the impedance level of the IF-load, rendering 2 times more voltage gain for the same supply headroom. The I/Q-BLIXER theoretically has only 1 dB less gain than a Balun-LNA biased at the same current. Also, its double side band noise figure is only 1–2 dB higher than for the Balun-LNA alone.

The I/Q-BLIXER topology implements Balun, LNA and I/Q down-conversion functionality, all in one circuit core. A 65nm CMOS implementation achieves >18 dB conversion gain, a flat NF <5.5 dB from 500 MHz to 7 GHz, IIP2 = +20 dBm and IIP3 = -3 dBm. The core circuit consumes 16 mW which is about 2 times lower than comparable wideband down-converters with I/Q-outputs. The area of the I/Q-BLIXER core occupies less than 0.01 mm^2 in 65nm CMOS, which makes it the smallest wideband down-converter design published.

Chapter 6

Discussion and recent publications

This chapter starts with a review of the three designs that are presented in Chapter 3 to 5. In section 6.1 the key performance points of these designs are discussed. Next to this, it is discussed how the designs evolve from to another and how they address the open or weaker points of the preceding design.

After this discussion, a review of recent publications on wideband LNAs is presented using a comparison table, in section 6.2. This table lists all the relevant properties of wideband LNAs and the designs of Chapter 3 and 4 are included to place them into perspective. The wideband frontend design of Chapter 5 is placed in context in a table comparing recent wideband frontend designs in section 6.3.

6.1 Discussion of the designs

In this section the CG-autotrafo-CS (Chapter 3), the Balun-LNA (Chapter 4) and the BLIXER (Chapter 5) designs are reviewed and their relation is discussed.

6.1.1 The CG-autotrafo-CS LNA

The CG-autotrafo-CS design of Chapter 3 was the first LNA designed in this project. Figure 6.1 shows the basic schematic of the CG-autotrafo-CS LNA. The name originates from the used common gate (CG) and common source (CS) stage in combination with an on-chip auto-transformer (autotrafo). An auto-transformer is a trans-

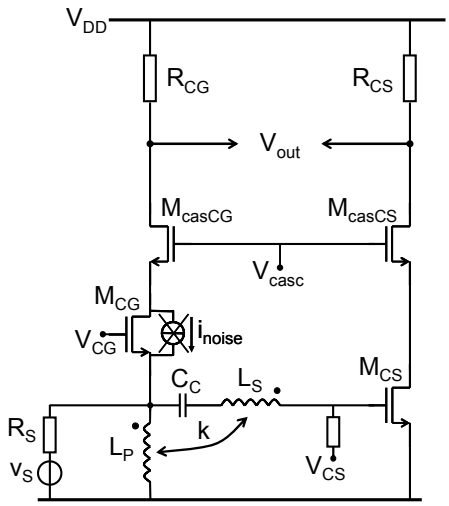

Figure 6.1: Basic schematic of the CG-autotrafo-CS LNA.

former where the primary and secondary inductors are stacked on top of each other.

In the CG-autotrafo-CS design, the CG-transistor provides input impedance matching, whereas its noise is canceled using the CS-path. In order to obtain a low noise figure, the noise contribution of the CS stage needs to be low. The noise in an amplifier stage can be reduced by scaling the impedances down. However, scaling down the impedance means that the transistor(s) need higher transconductance , which will increase power consumption. In the CG-autotrafo-CS design the on-chip transformer is used in the CS-path to mitigate high power consumption. The transformer provides passive voltage gain, which consumes no power and is in principle noise free. Although this transformer consumes considerable chip area, it is well spent. Next to providing power dissipation free voltage gain, the transformer is used for low-noise biasing the matching stage. Furthermore, its effective inductance resonates with the input capacitance, which provides matching in a high frequency band and filters of out-of-band signals.

The use of the on-chip transformer resulted in design with low power consumption (8 mW). Furthermore, it was the smallest wideband LNA in the multi-GHz range published at the time, requiring only one integrated inductor and no external components. There are however a few points that need to be addressed about this design.

The transformer in the CS-path also has some disadvantages. The input referred linearity (IIP3 and IIP2) of the CS-path is reduced by the voltage gain of the transformer, as the CS-transistor receives a larger input voltage. Furthermore, at the input of the transformer the input capacitance of the CS-transistor is transformed into a larger value, lowering the input bandwidth.

The circuit was designed for a noise figure in the order of 3 dB. However, the measurements showed a noise figure that was 1–2 dB higher than the expectations based on simulations. The reason(s) for the increased noise figure could unfortunately not be determined. There were indications that non-typical processing might be one of the reasons, as other designs processed on the same MPW also showed worse results than expected from simulations.

The measurements were carried out using wafer probing and parasitics of a package, such as bondwires and capacitances, were not taken into account. And although the design is wideband, the attained input bandwidth of 1.5 GHz (S_{11} < -10 dB between 2.5–4.0 GHz) is not high enough for SDR and full-bandwidth UWB applications. Next to this, the differential output signal was not optimized for balanced operation and the IIP2 of the circuit was not determined.

All these aspects, the noise figure, the package parasitics, balancing the output signal and achieving high linearity, were addressed in the second design, the Balun-LNA.

6.1.2 The Balun-LNA

The Balun-LNA design presented in Chapter 4 is shown in Figure 6.2. The focus of this design was to increase the bandwidth, obtain higher linearity and improve the balancing of the differential output signal compared to the CG-autotrafo-CS design.

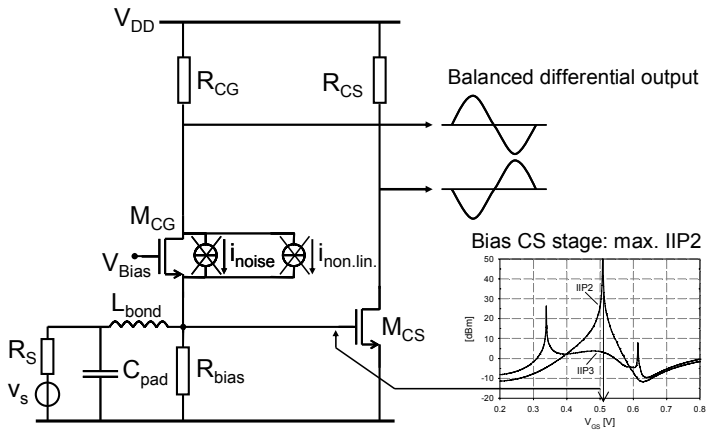

Figure 6.2: Basic schematic of the Balun-LNA.

Similar to the CG-autotrafo-CS, also the Balun-LNA design is based on the noise canceling CG-CS topology. The Balun-LNA has a single-ended input and a differential output, essentially implementing balun functionality. In contrast to designs that have a differential input an off-chip balun is not required to interface between the mostly single-ended antennas or band-filters and the chip input. The Balun-LNA design is completely inductorless and does not require any external components, which makes it a very compact design.

The Balun-LNA uses a different matching strategy than the CG-autotrafo-CS design. The CG-autotrafo-CS uses on-chip inductance to resonate with the input capacitance, which creates a resonance dip in the S_{11}. Instead, the Balun-LNA uses a low-pass matching strategy. To obtain large bandwidth, the input capacitance is kept low. Furthermore, the bondwire, which is always present in practice, is exploited to extend the input matching-bandwidth. The input capacitance, the bondwire and the external pad-capacitance form a broadband C-L-C-section, which extends the S_{11}-bandwidth.

Distortion caused by non-linearity of the CG (or matching) transistor is removed through distortion canceling. This distortion canceling can be exploited in any noise canceling topology. The key to obtain high overall linearity is to design a CS-stage with high linearity.

Especially low second order distortion can be obtained by biasing the CS-stage around its maximum in gain, yielding a wideband LNA with high IIP2.

In contrast to the CG-autotrafo-CS design the influence of bondwires is included, as the measurements on the Balun-LNA are carried out on a PCB with wirebonded chip in- and outputs.

Compared to the CG-autotrafo-CS design, larger bandwidth, lower noise figure, a well-balanced output signal and higher linearity is achieved, while the Balun-LNA is a much more compact design, occupying significantly less active area. This all comes at slightly higher power consumption (12 mW versus 8 mW).

The Balun-LNA design solves the problem of wideband, low-noise amplification with high linearity. Still, to implement a receiver down-conversion mixers (I & Q) need to be added behind the LNA. This presents challenges for both the bandwidth and the linearity. The capacitive loading of the mixer input stage(s) limits the bandwidth of the LNA-mixer combination. Especially for compact (inductorless) designs where peaking inductors in the LNA load are to be avoided. Next to this, the required linearity of the mixer input stage(s) is higher than for the LNA. Due to the voltage gain of the LNA, the mixers are driven with a larger input voltage.

These challenges on bandwidth and linearity of the LNA-mixer combination were addressed in the next design, the BLIXER.

6.1.3 The BLIXER

The next evolution of the basic CG-CS topology is the BLIXER, discussed in Chapter 5. The basic schematic of the I/Q- BLIXER is shown in Figure 6.3. This design combines the Balun-LNA and I&Q-mixers into a single topology. The key point in this design is that the signal is converted from high (RF) to low (IF) frequencies 'as quickly as possible,' i.e. using the least number of stages. In the BLIXER topology voltage gain at RF is avoided, instead the output currents of the CG- and CS-transistors are directly mixed-down to IF. By using this

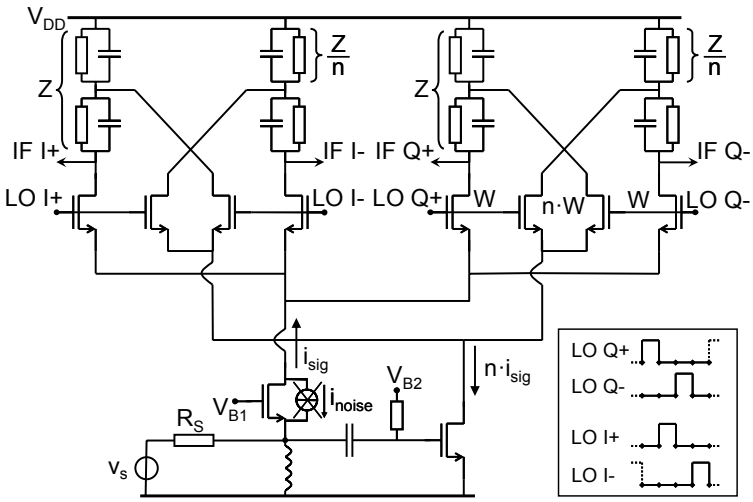

Figure 6.3: Basic schematic of the I/Q-BLIXER.

principle a compact receiver frontend with large bandwidth and high linearity is obtained.

The obtained bandwidth is large because there are no high-impedance nodes present in the RF-part of the design. High-impedance nodes can limit the bandwidth when they are capacitively loaded, especially when peaking inductors are to be avoided in order to keep the design compact. The BLIXER topology has only three nodes that carry the high-frequency (RF) signal, the chip-input and the two output nodes of the CG and CS-transistor. In the design these nodes are at an impedance level of 50 Ω or below.

The obtained linearity is high because only one V-to-I conversion at RF, the CS-transistor, determines the non-linearity. The distortion due to non-linearity of the CG-transistor is canceled. Furthermore, distortion due to the non-linear output impedance of the CS-transistor is low. Its drain-source voltage swing is low due to the low voltage gain at RF. In a traditional design there is a cascade of non-linear V-to-I conversions in the LNA-mixer chain, which will hamper linearity.

In contrast to the Balun-LNA, the BLIXER design requires an external inductor but it is used efficiently. Firstly this inductor provides a low-noise biasing of the CG-transistor without requiring any voltage-headroom. Saving voltage headroom is valuable as the BLIXER is a stacked topology. Secondly, the inductor is used for broadband input impedance matching. Its inductance sets the lower cut-off frequency of the input impedance match (S_{11}), a large inductance results in a low cut-off frequency. Furthermore, the normally inconvenient parasitic capacitance of the inductor is exploited. Together with the bondwire of the package and the parasitic input capacitance of the circuit it allows matching at high frequencies. Next to this, the external inductor makes it possible to (re-)use the chip in narrowband applications. The parallel LC-combination of the external inductor and input capacitance will determine the frequency band of operation and act as a band-filter. All this justifies the use of an external inductor. As an (narrowband) alternative the external inductor could be replaced by a bondwire.

The power consumption of the (I/Q)-BLIXER core is a bit higher than the power consumption of the Balun-LNA core (16 mW versus 12 mW). However, the BLIXER implements much more functionality, i.e. I&Q-mixing, for this slightly higher power consumption. Next to this, especially at high frequencies, often the local oscillator (LO) generation and buffering that are dominant in the overall power consumption of a receiver frontend, this is also true for the BLIXER.

The I/Q variant of the BLIXER (I/Q-BLIXER) requires an LO signal with 25% duty-cycle. In the implemented design the block that generates the multiple LO-phases (25% duty-cycle) does not operate at frequencies above 7 GHz. It remains a challenge to implement power efficient circuits that generate multiple phased, high frequency, LO signals.

In the BLIXER design, harmonic mixing is not investigated. Harmonic mixing [20, 70-71] occurs when unwanted mixing with the harmonics of the fundamental LO-frequency takes place. This can hamper the reception of the wanted signal when (large) interferers are present at frequencies around the LO-harmonics. In case reducing the interferer power around the LO-harmonics using filtering is not

possible or not sufficient, then the BLIXER topology might need to be adapted. One can think of splitting the design into multiple, scaled, parallel paths to obtain harmonic rejection as in [70].

Although there still are challenges with respect to the LO-generation and possible harmonic mixing, the I/Q-BLIXER topology is truly a compact wideband receiver frontend. The design is wideband as it operates from 0.5 up to 7 GHz and compact as it requires no off-chip balun, only one external inductor and no on-chip inductors.

6.2 Recently published wideband CMOS LNAs

As discussed in Chapter 2, only a handful of wideband CMOS LNAs were published before 2004. From 2004 and onwards, the number of publications on this topic has increased significantly. This section gives an overview of publications on wideband CMOS LNAs in the period form 2004 to 2009. To keep the number of publications within reasonable bounds, only publications in the IEEE Journal of Solid State Circuits (JSSC) are considered. Next to this, publications in the 2009 edition of the ISSCC, RFIC, ESSCIRC, CICC and VLSI conferences are taken into account, as these publications might still result in a JSSC paper at the time of writing this thesis.

Section 6.2.1 presents a table listing the relevant properties of the wideband LNAs. The different circuit techniques used in the LNAs and their performance are discussed in the section 6.2.2 to 6.2.6.

6.2.1 Table of wideband CMOS LNAs

Table 6-I shows the performance of the recent wideband CMOS LNAs. The table is spread across two pages in order to present the performance parameters of each LNA on a single row. The publications are grouped per circuit technique, the first part of Table 6-I on page 104 and 105 lists Input filter, Distributed amplifier and Common gate based LNAs. Negative feedback LNAs are listed on on page 106 and 107. In the last part of the table, on page 108 and 109, Noise Canceling LNAs are listed. Some publications describe a complete receiver. If sufficient measurement results of the (stand-alone) LNA are given, then the publication is included in Table 6-I.

The first column shows the reference and when and where the paper was published. The used circuit technique is given in the second column. Whether the LNA is single-ended, differential or that it has a single-ended input and a differential output (Balun) is listed in the configuration ('Config.') column.

Both the -3 dB bandwidth of the gain and the frequency range where S_{11} < -10 dB is shown under 'Bandwidth.' The effective frequency range is listed in the column 'Combined.' This is the frequency range where *both* the gain is within 3 dB from its maximal value *and* S_{11} < -10 dB. The maximal achieved gain is shown in the next column. This column either lists the S-parameter gain (S_{21}) or the voltage gain (A_V). Note that for a single ended LNA, with characteristic in- and output termination, the voltage gain is 6 dB higher than the S_{21}.

The achieved noise figure across the 'Combined' bandwidth is shown in the NF column. When the NF is specified for a different (often smaller) frequency range, then this is indicated in the column. The second order linearity (IIP2) and third order linearity (IIP3), are listed in the first two columns of the right page. Many papers state only the IIP3 and omit the IIP2, even tough second order distortion is important in wideband circuits. To the right of the linearity columns, two columns follow that list the power consumption of the core circuit and the used supply voltage (VDD). The supply voltage is underlined when a higher than standard supply voltage for the used CMOS process is used.

The number of used inductors is listed in the 'Inductors' column. Most on-chip inductors are spiral inductors that are optimized to obtain a high quality factor (Q) and require large area. When other types of on-chip inductors are used, such as stripline or low-Q inductors with small area, then this is noted in the column. Also off-chip inductors and external bias-Tees are counted. The 'Area' column shows the required circuit area of the core circuit, thus excluding the bondpads and other peripherals. When only the total chip area is given, then the circuit area is estimated based on the chip photograph. Finally, the last column states the used CMOS generation to implement the LNA.

TABLE 6-I
RECENT WIDEBAND CMOS LNAS – INPUT FILTER,

Ref.	Technique	Config.	Bandwidth [GHz]		Gain [dB]	NF [dB]
			$Gain_{-3dB}$ $S11_{-10dB}$	Combined		
JSSC Dec. '04 [72]	Input filter	Single ended	2.3–9.2 2.6–11.7	2.6–9.2	9.3 (S_{21})	4–7.5
JSSC Feb. '09 [73]	Input filter + output notch filters	Balun trnsformer at input	2.5–6 3–8.2	2.5–6	19 (A_V)	3.6–5.0 (3-5GHz)
JSSC June '06 [74]	Distributed amplifier	Single ended	0.04–7 0–7	0.04–7	8.6 (S_{21})	4.2–6 (0.5-6GHz)
JSSC Sept. '07 [75]	Distributed amplifier	Single ended	0.1–11 0-14	0.1–12	8 (S_{21})	2.9–4
ISSCC Feb. '09 [76]	Distributed amplifier	Single ended	0–12 0–12.5	0–12	15 (S_{21})	2.3–4.6 (1-11GHz)
JSSC Feb. '09 [77]	Common gate + lin. techn.	Single ended	1.5–8.1 2.8–12	2.8–8.1	11.7 (S_{21})	3.6–4.7
ISSCC Feb. '09 [78]	Common gate cross coupled +pos. feedback	Differ-ential	0.2–0.92 0.3–1.32	0.3–0.92	21 (A_V)	2–3.8

DISTRIBUTED AMPLFIER AND COMMON GATE DESIGNS

IIP2 [dBm]	IIP3 [dBm]	Power [mW]	VDD [V]	Inductors	Area [mm²]	Techno-logy
-3 – +6 (4–8GHz)	-8 – -6 (4–8GHz)	9	1.8	5	0.7 estimated	0.18µm CMOS
+28– +36 (2–6GHz)	+4.6 (5GHz)	32.5	1.5	5	1 estimated	0.13µm CMOS
?	+3 (2GHz)	9	1.3	8	1 estimated	0.18µm CMOS
?	-4.1 – -3 (1-10GHz)	21.6	1.8	11	0.4 estimated	0.18µm BiCMOS
?	-2 – +2 (1-11GHz)	26	1	17	0.27	0.13µm CMOS
+7.6 – +23	+11.7 – +14.1	2.6	1.2	3	0.3 estimated	0.13µm CMOS
?	-3.2 (0.7GHz)	3.6	1.8	2 off-chip	0.2 estimated	0.18µm CMOS

TABLE 6-I (CONTIUED)
RECENT WIDEBAND CMOS LNAS – NEGATIVE FEEDBACK DESIGNS

Ref.	Technique	Config.	Bandwidth [GHz]		Gain [dB]	NF [dB]
			$Gain_{-3dB}$ $S11_{-10dB}$	Combined		
JSSC Feb. '05 [44]	Negative feedback + ind. deg. CS	Single ended	2–4.6 3.1–6	3.1–4.6	9.8 (S_{21})	2.3–3.2
JSSC Sept. '05 [79]	Negative feedback + ind. peaking	Balun (not well balanced)	2–5.9 2.1–4.5	2.1–4.5	16 (S_{21})	4.7–5.8 (3-4.5GHz)
JSSC Nov. '06 [80]	Negative feedback + common gate	Differ-ential	0.05–0.93 0.05–0.9	0.05–0.9	13 (S_{21})	3.5–4.7
JSSC May '07 [81]	Negative feedback (reactive)	Single ended	1.5–11 3.5–10	3.5–10	17 (S_{21})	2–3
JSSC Nov. '08 [82]	Negative feedback	Single Ended	0–6.5 0–6.5	0–6.5	16.5 (S_{21})	2.7–3.5
JSSC Mar. '09 [83]	Negative feedback	Differ-ential	0.47–0.7 0.6–0.7	0.6–0.7	25 (A_V)	1.8
RFIC June '09 [84]	Negative feedback + ind. deg. CS	Single ended	0–29.5 0–22.1	0–22.1	10.7 (S_{21})	4.3–6.5 (0-15GHz)
RFIC June '09 [85]	Negative feedback + active balun	Balun	0.5–5.6 0.5-7	0.5–5.6	30 (S_{21})	3.6–4.3
RFIC June '09 [86]	Negative feedback	Balun	0.05–1 0.05–0.68	0.05–0.68	19.5 (S_{21})	2.4–4

1) Estimated using $P_{IIP3} = P_{1dB\,CP}$ + 9.6 dB [9]

IIP2 [dBm]	IIP3 [dBm]	Power [mW]	VDD [V]	Inductors	Area [mm²]	Techno-logy
?	-7	12.6	1.8	1 on-chip 2 off-chip	0.4 estimated	0.18µm CMOS
?	-12 [1)]	38	2	4 stripline 1 off-chip	0.24	0.13µm CMOS
?	-12 – -7	0.72	1.2	0	0.27	0.13µm CMOS
?	-7.2 – -4.3	9	1.2	3 + 1 bias-Tee	0.4 estimated	0.13µm CMOS
?	-7 – +1 (0.6–6GHz)	9.7	1.2	no	0.0017	90nm CMOS
?	-1	46.2	2.1	5	1.5	0.18µm CMOS
?	-6.1 – -2.7 (1–18GHz)	8.4	1.2	2 (1 stripline, 1 low-Q)	0.017	90nm CMOS
?	-24 (4GHz)	19	1.2	3	0.4 estimated	0.13µm CMOS
26	-2	35	1.8	no	0.042	0.18µm CMOS

TABLE 6-I (CONTIUED)
RECENT WIDEBAND CMOS LNAS – NOISE CANCELING DESIGNS

Ref.	Technique	Config.	Bandwidth [GHz] Gain-3dB S11-10dB	Bandwidth [GHz] Combined	Gain [dB]	NF [dB]
RFIC June '06 Chapt. 3	**Noise canceling**	**In: S.E. Out: Diff. unbalanced**	**1.8–5.4 2.5–4.0**	**2.5–4.0**	**19 (A_V)**	**4.0–5.4**
JSSC Dec '06 [20]	Noise canceling + ind. peaking	In: S.E. Out: Diff. unbalanced	0.8–6 ?	0.8–6	20 (A_V)	3–3.5 no graph.
JSSC Feb '07 [64]	Noise canceling + ind. peaking	Single Ended	1.2–11.9 0.2–14.0	1.2–11.9	9.7 (S_{21})	4.5–5.1 (3–10GHz)
JSSC May '08 [87]	Noise canceling	Single Ended	0.2–1.8 0.2–1.5	0.2–1.5	12 (S_{21})	2.6
JSSC June '08 Chapt. 4	**Noise canceling**	**Balun**	**0.1–5.0 0.1–6.1**	**0.1–5.0**	**15.6 (A_V)**	**3–4**
ISSCC Feb '09 [88]	Noise canceling	Balun	0.1–0.55 0.1–1	0.1–0.55	28 (A_V)	3.5–5
JSSC Mar. '09 [89]	Noise canceling	Single Ended	0.05–1.2 0.05–0.8	0.05–0.8	14 (S_{21})	3–4.5
JSSC Mar '09 [90]	Noise canceling + cross-coupl. CG	Balun	0.47–0.862 no graphs.		21 measured?	2.1 measured?

IIP2 [dBm]	IIP3 [dBm]	Power [mW]	VDD [V]	Inductors	Area [mm²]	Techno-logy
?	**-8**	**8**	**1.2**	**1 transformer**	**0.2**	**90nm CMOS**
?	-3.5 LNA+mixer	12.5	2.5	2	0.2 estimated	90nm CMOS
+10– +20 (3–6GHz)	-4.9 – -6.2 (3–6GHz)	20	1.8	5 + 1 Bias-Tee	0.59	0.18µm CMOS
?	+16 (max.)	17.4	1.5	no	0.1	0.13µm CMOS
+20	**0**	**14**	**1.2**	**no**	**0.009**	**65nm CMOS**
+ 28	+2.5	7.8	1.2	1 off-chip	0.075	90nm CMOS
+44	+3	34.8	2.2	no	0.16	0.18µm CMOS
?	0	3.6	1.2	1 off-chip	0.1 estimated	0.13µm CMOS

6.2.2 Input filter technique

The input filter technique extends the input bandwidth of an inductively degenerated common source LNA, which is a popular narrowband LNA topology. This technique was used for the first CMOS LNAs for UWB, published at the ISSCC in 2004 ([29], see section 2.3.2). An extended paper on this LNA was published in the 2004 December issue of the JSSC [72]. The first line of Table 6-I lists the achieved performance of this LNA. Indeed, this LNA achieves a large bandwidth. However, its noise figure is relatively high due to the losses of the LC-filter preceding amplification. Furthermore, requiring 5 integrated inductors the required circuit area is high.

The input filter topology published in [73] achieves high linearity by applying a notch filter at the output of the LNA which rejects strong out-of-band interferers. Furthermore, for low second order distortion the active part of the circuit is differential. An on-chip transformer at the input is embedded in the input-filter and simultaneously acts as a balun. Again, the required circuit area of this solution is high as 5 integrated inductors (transformers) are required.

6.2.3 Distributed amplifier

In the field of distributed amplifiers progress has been made towards lower area and lower noise figures. The distributed amplifier of [74] still had a relatively high noise figure (4.2–6 dB) and required about 1 mm^2 active area. Newer, more compact, distributed amplifiers with lower noise figures are published in [75-76]. These distributed amplifiers have however a relatively high power consumption (more than 20mW). The distributed amplifier of [76] is interesting as it uses a relative low circuit area (0.27mm^2), considering that 17 integrated inductors are used. In this design mutual coupling of inductors is exploited, resulting in relatively small inductors that are placed closely together.

The third order linearity (IIP3) of the distributed amplifiers in Table 6-I is acceptable, around 0 dBm. However, the IIP2 not mentioned in these publications. As single ended topologies are used

and no other measures for low second order distortion are taken, low IIP2 figures are expected.

6.2.4 Common gate based techniques

The common gate (CG) stage is a straight-forward circuit technique to provide a wideband input match. The real part of the input impedance is directly related to the transconductance of the matching transistor: $R_{in} = 1/g_m$. The minimum noise figure of a CG-stage is 2.2 dB, taking only thermal the noise of the input transistor into account and assuming a theoretical transistor noise excess factor (NEF or γ/α) of 2/3 [9]. In practice the noise figure of a CG-stage is higher as there are more noise sources than the thermal noise of the input transistor and the NEF is higher than 2/3 for short channel transistors.

In [77] a CG LNA is published which achieves good linearity by exploiting a linearization technique. The schematic of this LNA is shown in Figure 6.4 (left). A diode connected transistor (M1a) at drain of CG-transistor (partially) cancels its non-linear output currents. The achieved noise figure is low (~4 dB), certainly for a CG LNA at the reported low power consumption (2.6 mW). Unfortunately, not many details on the remarkable combination of noise figure and power

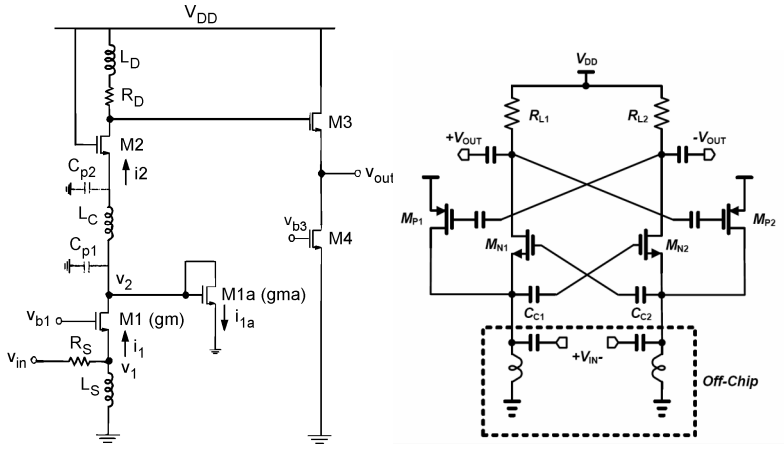

Figure 6.4: Common Gate LNAs of [77] (left) and [78] (right).

consumption are given, as the focus was more on achieving high linearity.

A differential CG LNA with cross-coupled CG-transistors is reported in [78] and shown in Figure 6.4 (right). Next to this, positive feedback from CG output to its input is applied to obtain low noise figure. Large capacitors are required for cross-coupling the CG-transistors. These capacitors occupy a large part of the circuit area and their parasitics limit the S_{11}-bandwidth.

6.2.5 Negative feedback

From 2004 to 2009, many papers were published on wideband LNA based on negative feedback. In most topologies a common source (CS) stage serves as input stage. The input stage is followed by one or two amplifying stages and (global) feedback is applied from the output of the last stage to the input node. Some topologies use passive, resistive feedback [79, 83], were others use transistors in the feedback circuit (active feedback) [82, 85-86]. Next to this, the inductively degenerated CS stage, known as a narrowband technique, is combined with feedback to broaden its input bandwidth [44, 84].

In [80] a cross-coupled common gate stage is combined with resistive feedback. The circuit has very low power consumption (0.72mW). It is designed for operation below 1 GHz, the use of cross-coupling capacitors limits the extension to larger bandwidths.

Reactive feedback, using on-chip transformers, is used in [81]. A low noise figure (2–3 dB) is obtained over a large bandwidth (3.5–10 GHz). However, for the measurements an external bias-T is used and the required circuit area is large as 2 transformers and 1 inductor are integrated on the chip.

A part of the title of [83], "… novel wideband impedance matching technique," attracts attention. However, the frequency range where S_{11} < -10 dB is not wideband (only between 0.6 – 0.7 GHz). Therefore, it can be questioned whether the term 'wideband matching technique' is justified. The circuit area is large and the low noise figure is merely

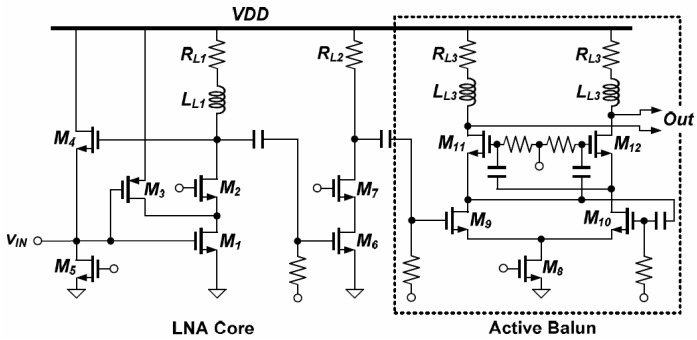

Figure 6.5: Negative feedback LNA cascaded with an active balun [85]

achieved by spending a lot of power, keeping the impedances in the amplifier low.

A negative feedback LNA cascaded with an active balun, shown in Figure 6.5, is presented in [85]. The balun consists of a differential pair with cross-coupled cascodes, which results in a well balanced differential output. Due to cascade of active circuits with gain, the linearity is relatively low (IIP3 = -24 dBm).

The LNA shown in Figure 6.6 obtains a higher 3rd order linearity [86]. Furthermore, this is the only publication of a negative feedback LNA that reports the IIP2. This paper shows that negative feedback can be combined with single-to-differential (balun) functionality. Using a differential-to-single converter ('Combiner'), the differential output signals are combined and fed back to the single-ended input. The circuit is designed for operation below 1 GHz, its power consumption relatively high (35 mW).

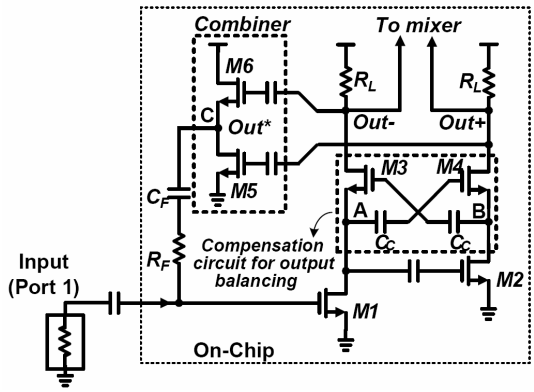

Figure 6.6: Negative feedback LNA with differential output [86].

The negative feedback amplifier design that is most suitable for the implementation of a "compact wideband receiver frontend" is presented in [82]. This article presents a narrowband, a multiband and a broadband version of the generic amplifier shown in Figure 6.7. The wideband version is included in Table 6-I. This wideband LNA covers the SDR frequency range (0–6.5 GHz), obtains low noise figure (2.7–3.5 dB) and reasonable 3rd order linearity (-7– +1 dBm), while consuming less than 10 mW. Furthermore, the inductorless design is the most compact wideband LNA found in literature (0.0017 mm^2). High second order linearity is not expected as it is a single-ended design and active, non-linear, feedback is used. Unfortunately, the obtained IIP2 is not mentioned in the article.

Based on the topology of Figure 6.7, the LNA presented in [84] achieves a bandwidth of 22 GHz. This large bandwidth is achieved by adding two inductors. A stripline inductor is added in the source of the input transistor (M_1), essentially creating an inductively degenerated common source stage. Another low area, low-Q inductor is added to obtain inductive peaking in the load (Z_{LOAD}). The noise figure and required area are higher (respectively 4.3–6.5 dB and 0.017 mm^2) than the design of [82], while its power consumption is in the same order.

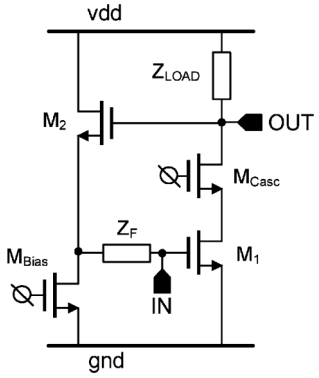

Figure 6.7: Generic feedback LNA of [82].

6.2.6 Noise canceling

Since 2004 the interest in the noise canceling technique has increased. This is apparent from the number of publications in Table 6-I on noise canceling wideband LNAs. Although the noise canceling technique does not rely on the use of inductors, many noise canceling LNAs do use inductors. One reason to use inductors is to extend the bandwidth at the output by using inductive peaking. Without using inductors, the bandwidth at the output of the LNA is RC-limited by the output resistor of the LNA and its loading capacitance. The bandwidth can be extended by applying an inductor in series with the output resistor. Another reason to use inductors is to achieve low-noise biasing, while requiring minimal voltage headroom.

The LNA published in [64] achieves the largest bandwidth (1.2–11.9 GHz) among the noise canceling LNAs. However, it requires significant circuit area (0.59 mm^2) as 5 integrated inductors are used. This LNA achieves reasonable linearity in the frequency range of 3-6 GHz (IIP2: +10 to +20 dBm and IIP3 ∼-5 dBm).

The Balun-LNA discussed in Chapter 4 achieves higher linearity (IIP2 = +20 dBm and IIP3 = 0 dBm). Furthermore, the Balun-LNA circuit includes balun functionality and the area is the lowest of the noise canceling topologies (0.009 mm^2).

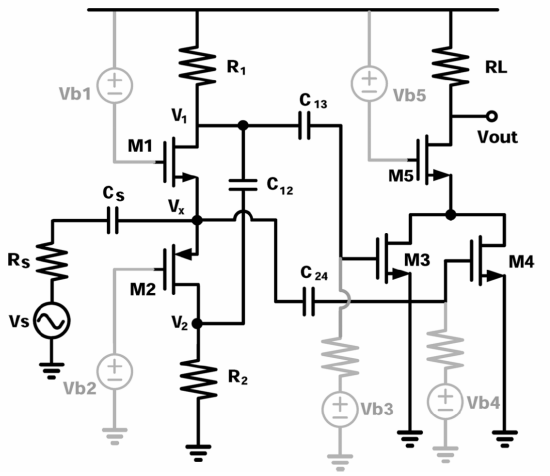

Figure 6.8: Noise canceling LNA of [87].

A noise canceling LNA with high linearity is published in [87] and shown in Figure 6.8. Distortion canceling of the matching transistors (M_1 and M_2), which is present in all noise canceling circuits, is exploited. Next to this, the size and biasing transistors M_3 and M_4 are optimized such that their 3rd order non-linearity cancels. A peak IIP3 of +16 dBm is obtained. The peak in IIP3 is sensitive to process spread and mismatch. This is emulated by varying bias voltage 'Vb3' around its optimal value, a 50 mV variation reduces the attained IIP3 to +5 dBm. A low noise figure of 2.6 dB is achieved. The second order linearity (IIP2) is not mentioned and the bandwidth is modest (1.5 GHz).

The most recent wideband noise canceling LNAs [88-90] are designed for digital TV (DVB-T, DVB-H, etc.). These LNAs are designed to operate at frequencies below 1 GHz. In [89] a single-ended wideband LNA is published that obtains a very high IIP2 (+44 dBm). In this design low second order distortion is obtained by using complementary NMOS and PMOS stages. Taking process spread into account the minimal IIP2 is in the order of +36 dBm.

6.2.7 Conclusions on overview of wideband CMOS LNAs

The number of publications on wideband amplification for receivers from 2004 though 2009 shows that this topic has received much attention over the last years. Based on the publications two techniques seem most suitable for the implementation of compact wideband receiver frontends: Negative feedback and Noise canceling. Input filter and Distributed amplifier techniques generally require too many integrated inductors to yield compact designs.

The CG-autotrafo-CS LNA of Chapter 3 was targeted and achieves low power consumption compared to other designs. Only a few multi-GHz LNAs have lower power consumption. The other performance metrics (NF, linearity, area) of the CG-autotrafo-CS LNA are fair but not exceptional when compared to other designs in Table 6-I.

The Balun-LNA compares more favorably with other designs. The achieved bandwidth is suitable for SDR operation as the frequencies of most wireless communication standards are covered. The Balun-LNA is the smallest (0.009 mm^2) of the Noise canceling LNAs and only one Negative feedback based LNA [82] occupies lower circuit area. Compared to this LNA the Balun-LNA has more functionality as it also provides single-ended to differential conversion. The second order linearity (IIP2) is among the highest reported for LNAs operating above 1 GHz. The Input filter based LNA of [73] achieves higher IIP2. However, as it relies on the use of on-chip transformers and inductors it requires significantly more circuit area (~1 mm^2). The 3rd order linearity of the Balun-LNA is not the highest but it is among the highest reported. The power consumption is in the lower range of the reported values. The Balun-LNA uses the standard supply voltage for the used technology (1.2 V for CMOS 65nm), other designs use higher than standard supply voltages [20, 73, 79, 83, 87, 89].

The published LNAs in Table 6-I obtain wideband amplification. However, this is only one part of the wideband frontend puzzle. In a receiver the signal also needs to be brought down to low frequencies. Obtaining large bandwidth and linearity in a LNA-mixer combination, while keeping the noise at an acceptable level, is a challenge that is

addressed by the wideband receiver frontends discussed in the next section.

6.3 Recently published wideband receiver frontends

This section gives an overview of wideband CMOS receiver frontends published in the period 2004 to 2009. As in section 6.2, only publications from the IEEE Journal of Solid State Circuits and the 2009 edition of the ISSCC, RFIC, ESSCIRC, CICC and VLSI conferences are considered. The BLIXER topology, described in Chapter 5, is one of these wideband frontends.

6.3.1 Table of wideband CMOS receiver frontends

Table 6-II gives an overview of the recently published wideband CMOS receiver frontends. This table is used to benchmark the BLIXER design presented in Chapter 5. Most wideband frontends use one of the RF circuit techniques discussed in section 6.2 to obtain low-noise wideband amplification and input matching. The used RF circuit technique can be found in the second column of Table 6-II.

The circuit configuration is mentioned in the third column. This column shows whether the receiver has a single-ended or a differential input and whether it has in-phase and quadrature (I&Q) mixer-outputs or that it has only one output (I-path). All receivers in Table 6-II provide differential signals at the mixer output(s).

The receivers in the table are sorted from small to large RF-bandwidth, which is shown in the fourth column (the number within brackets).

The maximal achieved conversion gain from RF to IF, which can vary over the band, is placed in the fifth column. When an IF-amplifier is used then this is noted in the column. The noise figure is placed in the next column, for most receivers this is the double sideband (DSB) noise figure. When only the single sideband (SSB) noise figure is given, then this is put as a note in the column.

All except one publication report the third order linearity (IIP3). The second order non-linearity (IIP2) is often not mentioned, even though it is very important for wideband receivers. For the IIP2 two figures are given, the 'RF-to-RF' and the 'RF-to-IF' IIP2, shown in the first two columns on the right half of Table 6-II.

The 'RF-to-RF' IIP2 describes the second order linearity of the part of the receiver that carries the RF-signal, i.e. the part up to, and including, the mixer input. This specification is typical for wideband receivers. In narrowband receivers these 2nd order intermodulation products will always fall out of the RF-band of interest.

The 'RF-to-IF' IIP2 reports the level of the non-linear terms that are generated in the RF part of the receiver and subsequently leak though the mixer to end up in the IF-band, as explained in section 2.2.5. If an article reports only one IIP2 figure, it is in most cases the 'RF-to-IF' IIP2. This is probably because only the 'RF-to-IF' IIP2 is of importance in traditional narrowband receivers.

The column 'Power' gives the power consumption of the receiver frontend core, i.e. the LNA plus mixer(s). Footnotes indicate when LO-buffers, LO I/Q-phase generation[1], IF-amplifiers or a PLL is included in the power consumption. Furthermore, it is noted when the power consumption is for the complete receiver (Rx), or even for the complete transceiver (Rx & Tx).

The next column shows the used supply voltage (VDD), some publications use a supply higher than standard supply voltage of the used CMOS technology, these cases are underlined. The column showing the number of inductors that are used in the receiver path (Rx-path) and the column that gives the required area of the receiver are placed next to each other, as they are strongly related. The last column shows the generation of CMOS technology that is used to implement the receiver.

[1] The LO I/Q-phase generation is in most cases a divide-by-two circuit. In some cases, when more LO-phases are required, a slightly more complicated circuit is used.

TABLE 6-II
RECENT WIDEBAND CMOS RECEIVER FRONTENDS

Ref.	RF Technique	Config.	RF Band (BW) [GHz]	Conversion gain (max) [dB]	NF [dB]	IIP3 [dBm]
JSSC Dec. '09 [70]	CG & CS combination; no A_V at RF	In: diff. Out: I&Q	0.4–0.9 (0.5)	34 incl. IF-Amp	3.5–4.4	+3.5 Out band: +16
JSSC Apr. '06 [91]	Common gate with positive feedback	In: diff. Out: I&Q	1.5–2.5 (1.0)	24–30	5.2–5.8	-7.5 – 0
JSSC Apr. '08 [92]	Input filter	In: S.E. Out: I&Q	3.3–4.8 (1.5)	57 incl. IF-Amp	4.5–5.4	-10 – -5
JSSC Dec. '05 [93]	Common gate, switchable inductive load	In: S.E Out: I&Q	2.8–4.5 (1.7)	69–73 incl. IF-Amp	6.5–8.4	-20 [1)]
JSSC Dec. '06 [94]	Input filter phased-array (dual-antenna)	In: diff (2) Out: I&Q	3.1–4.8 (1.7)	63–64 incl. IF-Amp	4.0–4.7	-0.8– +4.2 @min. gain
JSSC Dec. '06 [95]	Negative feedback	In: S.E. Out: I&Q	3.1–4.8 (1.7)	36–37	3.6–4.1	-22
JSSC Feb. '09 [73]	Input filter +output notch filter	In: S.E. Out: I&Q	3.1–4.8 (1.7)	20–25	5.1–6.2	-20 [1)]; Out band: -5 – -2
ISSCC Feb. '09 [96]	QSM, LNA-less no 50Ω match no A_V at RF	In: diff. Out: I&Q	0.2–2 (1.8)	19	5–6.5	+11
RFIC June '09 [97]	Negative feedback	In: diff. Out: I&Q	0.3–2.6 (2.3)	39–43 incl. IF-Amp	2.3–4.1 deembed.	-6.5 – +4

[1)] Estimated using $P_{IIP3} = P_{1dB\,CP} + 9.6$ dB [9]

IIP2 [dBm]		Power [mW]	VDD [V]	Inductors in Rx-path	Area [mm²]	Techno-logy
RF-to-RF	RF-to-IF					
?	+46	60 a , b, c	1.2	2 off-chip	0.8 estimated	65nm CMOS
?	+50 – +54	24	1.2	4 on-chip 2 off-chip	1.5	0.13µm CMOS
?	?	67 a, c	1.8	4	1.2 estimated	0.18µm CMOS
?	?	105 e	1.5	4	<1	0.13µm CMOS
?	+22 – +25 @min. gain	527 f	1.8	10 (2 × 5)	3 estimated	0.18µm CMOS
?	?	51 a?	1.5	4	0.7 estimated	0.13µm CMOS
+6– +20	?	31–36	1.5	5	2 estimated	0.13µm CMOS
?	+65	67 a, b	1.2	no	0.13	65nm CMOS
?	+48	48–53 a, b	1.5	no	0.7	0.13µm CMOS

(a) incl. LO-buffer (b) incl. LO I/Q-phase gen. (c) incl. IF-amplifier
(d) incl. PLL (e) Complete Rx (f) complete Rx & Tx

TABLE 6-II (CONTINUED)
RECENT WIDEBAND CMOS RECEIVER FRONTENDS

Ref.	RF Technique	Config.	RF Band (BW) [GHz]	Conversion gain (max) [dB]	NF [dB]	IIP3 [dBm]
JSSC Aug '06 [98]	Common gate with positive feedback	In: S.E. Out: I&Q	3.1–4.8 6.3–7.9 (3.3)	20–23	5.2–7.7	-3.5 – +1
JSSC Feb. '07 [69]	CG & cross-coupled CS; no A_V at RF	In: diff. Out: I only	0.1–3.85 (3.8)	20	8.4–11.5 SSB	-3.2 [1] 2.3 GHz
JSSC May '08 [99]	Negative feedback	In: diff. Out: I only	2–5.8 (3.8)	44 incl. IF-Amp	3.4–3.9	-7 – -4
JSSC Mar. '07 [100]	Negative feedback	In: diff IF-Out: 2.64 GHz	3.1–7.9 (4.8)	15–20	5–6.6	-7– -3
ISSCC Feb. '09 [101]	Negative feedback	In: S.E. Out: I&Q	0.1–5 (4.9)	84 incl. IF-Amp	2.3–6.5	-11 – -4
JSSC Feb. '09 [102]	Common gate cross coupled	In: diff. Out: I&Q	3.1–8.0 (4.9)	81–88 incl. IF-Amp	6.5–8.3	-13 @min. gain
JSSC Dec. '06 [20]	Noise canceling	In: S.E. Out: I&Q	0.8–6 (5.2)	36 incl. IF-Amp	5 / 5.5 0.9/2.5GHz	-4 @mid. gain
JSSC Dec. '08 [103]	Negative feedback	In: S.E. Out: I only	0–6 (6)	26–31	4.5–6.8	-29 / -22 2 / 5 GHz
JSSC Dec. '09 [104]	Negative feedback inverter based	In: S.E. Out: I&Q	3–9 (6)	55–58 incl. IF-Amp	4.5–5.5	-2 – -4

[1] Estimated using $P_{IIP3} = P_{1dB\,CP}$ + 9.6 dB [9]

IIP2 [dBm]		Power [mW]	VDD [V]	Inductors in Rx-path	Area [mm²]	Techno-logy
RF-to-RF	RF-to-IF					
+21	+35 – +46	18	1.8	3 on-chip 1 off-chip	0.7 estimated	0.18µm CMOS
?	?	9.8	1.2	4	0.88	90nm CMOS
?	?	76 (a: 89)	2.7	no	0.2	90nm CMOS
+33?	?	45	2.3	5 bondwires	0.35 incl. IF-BPF	0.18µm CMOS
?	+30 – +36	54–105 e	1.1	5? low-Q, small	0.3 estimated	45nm CMOS
+22 @min. gain	?	182 a?	1.8	11	2 estimated	0.18µm CMOS
?	+60 @mid. gain	44.5	2.5	2	0.5 estimated	90nm CMOS
?	?	40–50 a, b, d	1.2	no	0.06	90nm CMOS
?	?	156 a, b, d	1.2	no	0.2 estimated	65nm CMOS

(a) incl. LO-buffer (b) incl. LO I/Q-phase gen. (c) incl. IF-amplifier
(d) incl. PLL (e) Complete Rx (f) complete Rx & Tx

TABLE 6-II (CONTINUED)
RECENT WIDEBAND CMOS RECEIVER FRONTENDS

Ref.	RF Technique	Config.	RF Band (BW) [GHz]	Conversion gain (max) [dB]	NF [dB]	IIP3 [dBm]
ESSCIRC Sept. '09 [105]	Negative feedback	In: diff. Out: I only	2.1–8.2 (6.1)	20	5.9–7.5	-12 – -8
JSSC May '09 [106]	Distributed amplifier	In: S.E. Out: I&Q	3.1–9.5 (6.4)	22.6	?	?
JSSC Dec. '08 Chapt. 5	**Noise canceling; no A_V at RF**	**In: S.E. Out: I&Q**	**0.5–7 (6.5)**	**18**	**4.5–5.5**	**-3**
ESSCIRC Sept. '09 [107]	Noise canceling	In: diff. Out: I&Q	3–10 (7)	24–29	4.9–8.8	-13.5
RFIC June '09 [108]	Common gate cross coupled	In: diff. Out: I&Q	1–10 (9)	20	4.8–5.6	0

IIP2 [dBm]		Power [mW]	VDD [V]	Inductors in Rx-path	Area [mm²]	Techno-logy
RF-to-RF	RF-to-IF					
?	?	47	1.2	no	0.05	65nm CMOS
?	?	24 (a, b: 46)	1.2	5	0.6 estimated	90nm CMOS
+20	**+40**	**16 (a,b: 20–44)**	**1.2**	**1 off-chip**	**0.02**	**65nm CMOS**
?	+24	35	1.5	5	0.4 estimated	0.13µm CMOS
?	?	21 (a, b: 30)	1.2	2 off-chip bias&balun	0.039	0.13µm CMOS

(a) incl. LO-buffer (b) incl. LO I/Q-phase gen. (c) incl. IF-amplifier
(d) incl. PLL (e) Complete Rx (f) complete Rx & Tx

6.3.2 Circuit techniques in wideband receiver frontends

To obtain low-noise, wideband, amplification most frontends use one of the circuit techniques described in section 6.2:

- Input filter,
- Distributed amplifier,
- Common gate,
- Negative feedback,
- Noise canceling.

There are a few frontends that use a different circuit technique, which can not be classified in one of the techniques listed above.

In [70], on the top of Table 6-II, pseudo-differential common gate and common source transistor stages are used to convert the RF-input signal into an RF-current. This current is subsequently converted to IF by mixers. Similar to the BLIXER (Chapter 5) this receiver has no voltage gain at RF. The receivers that have this property have a note in the Technique column: 'no A_V at RF.' Furthermore, high out-of-band linearity is obtained by first applying low-pass filtering at IF before making voltage gain. In contrast to the BLIXER, this design has only partial noise canceling of the CG transistor noise. However, it does incorporate a harmonic-rejection (HR) technique, which is not present in the BLIXER design. The HR technique makes the receiver less sensitive to interference around the harmonics of the local oscillator (LO) signal.

The LNA-less design of [96] uses a Quadrature Sampling Mixer (QSM) which is connected directly at the input of the chip. The combination of low duty-cycle switching (25% max.), using quadrature signals, and holding the sampled value on a capacitor, results in a low noise figure and conversion loss (both 0.9 dB theoretically). Although the technique is quite different than the BLIXER, it has in common that there is no voltage gain at RF, and consequently a high linearity is obtained. A disadvantage of the design in [96] is that it provides no (50 Ω) input match. This may restrict its usage in a complete transceiver design where transmission-lines are used to distribute RF-signals from the antenna, filters, RF-switches and balun

to the input of the chip. A recent publication [109] using the same technique shows that it is possible to obtain a matched input impedance by tuning baseband (IF) resistors.

Another circuit technique is presented in [69] (in Table 6-II on the second row of page 122-123). The title of this work is "A 90-nm wideband merged CMOS LNA and mixer exploiting noise cancellation." The title suggest that this design is very similar to the BLIXER as it also uses noise canceling (or: cancellation) and a merged LNA-mixer. Indeed, this topology shares an important property with the BLIXER; it also has no voltage gain at RF. However, there are also quite some differences. The LNA-part of [69] consists of a two (pseudo-differential) common gate (CG) transistors on top of two cross-coupled common source (CS) transistors. In contrast to the BLIXER it has a differential input and the design only renders partial noise canceling of the CG transistor noise. It has a single mixer core and therefore no in-phase and quadrature (I&Q) IF-outputs. Instead of stacking the mixer on top of the LNA core, as in the BLIXER, a folded cascode structure is used in the LNA-mixer interface. Four current sources are required for the folded cascode structure, which are all degenerated by inductors to improve there noise behavior. Despite the use of (area consuming) inductors the obtained noise figure is higher than the NF achieved by the BLIXER[1]. The core power consumption is lower, however for a frontend with I and Q outputs it will have higher power consumption. The bandwidth of the conversion gain is smaller than the BLIXER-bandwidth. Furthermore, not much detail on the measured linearity is given, only a 1 dB-compression point at a single frequency is mentioned.

6.3.3 The BLIXER compared to other wideband receivers

In this section the properties and performance of the BLIXER compared to other wideband receivers will be discussed per parameter, i.e. per column of Table 6-II. The BLIXER properties are marked bold in Table 6-II and can be found at the third last row on page 124 and 125.

[1] The double sideband (DSB) NF that can be obtained is maximally 3 dB lower than the single sideband (SSB) NF reported in [69], see [9].

RF circuit technique

The BLIXER topology is based on the noise canceling technique. In contrast to the wideband LNAs discussed in section 6.2, not many wideband receivers based on the noise canceling technique have been reported; so far only two other receivers [20, 107].

Circuit configuration

The BLIXER, or to be more precise: the I/Q-BLIXER, is a wideband receiver with in-phase and quadrature IF-outputs. I and Q-outputs are required to implement a low- or zero-IF receiver. There are quite some papers that present a receiver with only one mixer. Extending these topologies to an I/Q topology without reducing the claimed single-mixer performance, in terms of bandwidth, linearity and power consumption, is not always straightforward.

RF-band of operation (RF-bandwidth)

The entries in Table 6-II are sorted from small to large bandwidth (the number within brackets in the 'RF-Band' column). Clearly, the BLIXER is one of the most wideband receivers, as it is the third last entry of the table. However, some receivers that have smaller bandwidth do operate on higher frequencies, which is especially important for UWB receivers.

At the upper bound of the of the RF-band (7 GHz) of the BLIXER, the conversion gain has dropped only 1 dB. The RF-band is thus not set by the -3 dB-point of the conversion gain, as is the case for many other receivers. Rather, the upper bound RF-band of the BLIXER is determined by both a peripheral LO-generation circuit (a 25% duty-cycle generator stops working at high frequencies) and the S_{11} bandwidth. The issue with the LO-generation can be solved by a re-design of this block. The S_{11} bandwidth can be extended by using packages with lower parasitics and by using more sophisticated package modeling. This would allow the extension of the RF-band of the BLIXER to the upper boundary of UWB (10.6 GHz).

Conversion gain

The conversion gain of the BLIXER is high enough to suppress noise of subsequent IF-amplifiers. The conversion gain is comparable to other designs that specify the conversion gain excluding the IF-amplification.

Noise figure

The noise figure of the BLIXER is slightly lower than the mean of the noise figures in Table 6-II. Furthermore, the noise figure of the BLIXER is quite flat (±0.5 dB) considering its large bandwidth (6.5 GHz).

Linearity

The third order linearity is in the higher range of reported IIP3s. For second order linearity there is only one other publication [98] that reports both the RF-to-IF IIP2 *and* the RF-to-RF IIP2. The receiver in [98] achieves a slightly higher linearity at the expense of a very large circuit area (about 35 times larger than the area of BLIXER). The RF-to-RF IIP2 of the BLIXER is among the highest of the designs that report this figure. For receivers with a single-ended input the RF-to-IF IIP2 is among the highest. Some differential input receivers achieve 10-20 dB higher values, but in these receivers an external balun is required.

Power consumption

The stacked LNA-mixer configuration of the BLIXER makes current re-use possible, which yields very low core power consumption (16 mW) compared to other designs. One other 'merged' LNA-mixer topology [69] has even a lower power consumption (9.8 mW). However, the BLIXER outperforms this design in terms of bandwidth, noise figure and circuit area.

In the BLIXER design, the power consumption of the LO-buffers that drive the mixers is higher than the core power consumption. This is seen in most other design as well, especially for designs operating at high frequencies. The power consumption of the LO-buffers and the 25% duty-cycle I/Q-phase generator circuitry depends on the frequency of operation as dynamic, inverter based, circuits are used. The power consumption of the BLIXER including the LO-buffers and phase

generator, is lower than other designs for low frequencies and comparable to other designs at the higher frequency range.

Supply voltage

The BLIXER operates on the standard supply voltage (1.2 V) of the 65nm CMOS process used for fabrication. Using the standard supply voltage is convenient for the integration of the receiver into a larger system, such as a SoC or a multi-chip module. Some other receivers operate using higher than standard supply voltages (the underlined figures). These designs require special thick-oxide transistors or careful circuit design in order to keep the expected device degradation at an acceptable level. Elevated supply voltages are used in order to obtain higher performance. Especially for gain and linearity, higher supply voltages could be beneficial. However, designs operating on higher than standard supply voltages do not show significant better performance than the BLIXER.

Circuit area

The circuit area of the BLIXER is so far the smallest wideband receiver frontend published. The area of the core circuit is smaller than 0.01 mm^2, while the area including the LO-buffering and 25%-duty-cycle LO-generation circuitry, required for I/Q-operation, is below than 0.02 mm^2, which is still two times smaller than the next smallest design [108]. Just as in [108], the absence of on-chip inductors makes very compact receiver designs possible.

Technology

All reported wideband frontends are fabricated in either 0.18µm, 0.13µm, 90nm, 65nm and one in 45nm [101][1] CMOS. The BLIXER is designed in a baseline digital 65nm CMOS process, without any analog/RF add-ons, such as thick top-metals for high Q-inductors or MiM-capacitors.

[1] This is not the first wideband frontend in 45nm CMOS; at the ISSCC 2008 "A 0.6-10GHz receiver front-end in 45nm CMOS" was published [110].

6.4 Conclusions

Judging by the number of publications there has been a large interest in wideband CMOS LNAs and receiver frontends in recent years.

A number of different techniques are used to implement wideband LNAs, but only two result in *compact* wideband LNAs: Negative feedback and Noise canceling.

From the two LNA designs of Chapter 2 (CG-autorafo-CS LNA) and Chapter 3 (Balun-LNA) especially the Balun-LNA compares favorably to other designs. It is the second smallest design, while providing more functionality (Balun) than the smallest design. The achieved bandwidth is suitable for SDR-operation. The noise figure and power consumption are among the lowest reported, while the linearity is in the higher range of the reported values.

The BLIXER design form Chapter 5 stands out on area and RF-bandwidth when compared with other wideband receiver frontends. The linearity is among the highest, while the noise figure is moderately-low and flat across the RF-band. The core power consumption of the BLIXER is low as the mixers are stacked on top of the LNA and bias current is reused.

The BLIXER topology truly is a compact wideband receiver frontend. It a is wideband design as it operates from 0.5 up to 7 GHz. Furthermore, it is a compact design as no off-chip balun, only one external inductor and no on-chip inductors are required.

Chapter 7

Conclusions

7.1 Conclusions

The desired properties of wideband receiver frontends are derived in Chapter 2. Wideband receivers have similar requirements on gain, input matching and noise figure as traditional narrowband receivers. As the name suggest, the difference is the *bandwidth* across which these specifications need to be met. As most existing circuit techniques used in receivers are narrowband, new circuit techniques are desired to implement wideband receivers.

Obtaining high linearity in wideband receivers is important, as pre-filters may be removed or their specifications relaxed. The third order linearity of wideband receivers needs to be at least as good as in narrowband receivers and preferably better. Wideband receivers have, similar to narrowband receivers, a requirement on the 'RF-to-IF' second order linearity. Next to this, wideband receivers have an additional requirement, the second order linearity of the RF-part, or 'RF-to-RF' linearity.

At the start of the project two circuit techniques, negative feedback and noise canceling, were seen as candidates to implement compact wideband receivers. Noise canceling was chosen in this project as it was a new technique which was deemed promising. The fact that it is a new and less explored technique makes noise canceling an interesting subject for research.

In [11] the noise canceling technique is explored and possible noise canceling topologies are given. A very interesting noise canceling topology is the Common-Gate Common-Source (CG-CS) topology. Compared to other noise canceling topologies it has an attractive noise performance. Furthermore, it has a single-ended input and a differential output, allowing the elimination of an off-chip balun.

The combination of the CG-CS topology and a transformer results in an area efficient, low-power noise canceling LNA (Chapter 3). At the time of publication the 'CG-autotrafo-CS LNA' was the smallest and most low-power LNA operating in the multi-GHz range. However, its noise figure is relatively high and the transformer at the input limits the bandwidth and linearity that can be achieved with this transformer based topology.

The CG-CS topology is used to implement a Balun-LNA that simultaneously yields noise canceling, distortion canceling and single-ended to, well-balanced, differential conversion (Chapter 4). High overall linearity can be obtained by exploiting an optimum in the linearity of the CS-stage, as the distortion of the CG-transistor is canceled. The Balun-LNA design is very competitive in terms of output balancing, noise figure and linearity when compared to other designs (Chapter 6). At the time of writing, there is only one LNA found that occupies lower area [82]. However, this is a single-ended LNA without balun functionality.

From the overview and comparison of wideband LNAs in Chapter 6 it follows that there are two circuit techniques suitable for the implementation of LNAs for *compact* wideband frontends: negative feedback and noise canceling. In contrast to other circuit techniques, these two circuit principle do not rely on the use of (high quality) inductors in order to obtain large bandwidth and low noise.

The BLIXER topology, described in Chapter 5, is a further evolution of the CG-CS topology. The (I/Q-)BLIXER topology implements Balun, LNA and I/Q down-conversion functionality, all in one circuit core.

The power consumption of the BLIXER core is low as the mixers, are stacked on top of the LNA-core. Hence, the mixers that implement

I/Q-mixing and require no additional bias current on top of the current required for the LNA functionality. The power consumption of the local oscillator (LO) buffering and phase generation circuits is frequency dependent as dynamic, inverter based, circuits are used. At high frequencies, the power consumption of these LO-circuits dominates over the core power consumption.

The noise figure of the BLIXER is low and flat across a large bandwidth by applying noise canceling, where the noise of the matching transistor is canceled at the mixer output.

Large bandwidth and high linearity are obtained by avoiding voltage gain at high frequencies. Instead, voltage gain is generated at low frequencies (IF), after the down-conversion by the mixer-core. The real part of the impedance (resistive part) of the nodes carrying RF-signals is low. This allows obtaining large bandwidth, without requiring on-chip inductors. As no on-chip inductors are required, a compact wideband frontend is obtained.

In contrast to traditional designs, a cascade of non-linear V-to-I conversions is avoided in the BLIXER. The output current of LNA core is absorbed by the mixers stacked on top of the LNA core. In principle only one high frequency V-to-I conversion determines the linearity, this makes high linearity possible.

Using the BLIXER topology, compact wideband receiver frontends can be implemented. From the comparison of the BLIXER to other wideband frontends (Chapter 6) it follows that its noise figure, linearity performance and power consumption are very competitive.

As defined in Chapter 1, one aim of this Ph.D. project was to ***explore the noise canceling technique for wideband applications***. This aim is obtained by the design and implementation of two wideband LNAs and one wideband receiver frontend and analyzing their performance. The Balun-LNA described in Chapter 4 uses the, at time already known, noise canceling CG-CS topology. However, it was the first design based on this topology that, next to noise canceling, explicitly exploited distortion canceling, while simultaneously achieving a well-balanced output signal. Next to this, the CG-autotrafo-

CS LNA described in Chapter 3 and the BLIXER of Chapter 5 are new topologies. Especially the BLIXER topology is suitable for the implementation of wideband receivers in CMOS and addresses the second part of the project goal, to ***develop wideband receiver circuit topologies in CMOS***.

7.2 Original contributions

The main original contributions in this thesis are:

The proposal of a new CG-autotrafo-CS noise canceling stage, which renders "passive voltage gain," reducing power consumption of the CS-stage.

The concept of simultaneous noise cancellation, distortion cancellation and a balanced differential output.

Analysis and optimization of the second order distortion of a resistively loaded CS-stage. Calculation of the optimum IIP2 taking into account not only the non-linearity of the transconductance but also non-linearity of *output impedance* and $v_{ds} \cdot v_{gs}$ cross-terms of deep sub-micron MOS transistors.

The proposal of the new BLIXER topology which avoids voltage gain at RF in order to achieve large bandwidth and linearity.

7.3 Recommendations for future research

At high frequencies, the distribution and buffering of the local oscillator (LO) signal often dominates the power consumption of a receiver. Next to this, new receiver topologies like the BLIXER and topologies incorporating harmonic rejection (HR) techniques [70-71] require specific phased LO-signals. In the BLIXER LO-signals with 25% duty-cycle are used and the HR topology of [70-71] requires 8 LO-signals with equidistant phases. Generation of these specific phased LO-signals becomes a challenge at high frequencies due to the delays in the circuitry. Research directed to find circuit topologies for the generation of multi-phase LO-signals suitable for high frequency

operation is useful, including high frequency power efficient LO-buffering.

Extending the BLIXER topology with harmonic rejection [70-71] is recommended because this would reduce its sensitivity to out-of-band interferers, relax the band-filter specifications, and yield a more versatile receiver. Both the BLIXER topologies and the HR technique rely on specific, multiple phased LO-signals. It is likely that circuit topologies can be found where the LO-phases required for HR can be reused for (I/Q)-BLIXER operation.

It is common practice to design circuits, and to be more specific for this thesis: receivers, for worst-case conditions. A worst case condition for a receiver is for example the reception of a very weak wanted signal in the presence of strong interfering signals. However, worst-case conditions occur seldom in practice. The result is that for most situations, i.e. for '99% of the time', the receivers are over-dimensioned and generally consume too much power. The solution to this would be circuits that 'know' the conditions (weak or strong wanted signal? interferers present?). Based on these conditions the circuit parameters, noise figure, linearity, etc. can be adapted to minimize power consumption. To allow the implementation of these 'adaptable receivers,' research is required to find systems that are capable of gathering information about the operation conditions. An important research area in this respect is the cognitive radio field. Next to this, is seems useful to aim at circuit topologies which can trade noise and linearity performance for power consumption, while maintaining high frequency of operation.

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Stephan C. Blaakmeer was born on 4 august 1976 in Stiens, The Netherlands. He received the M.Sc. degree in Electrical Engineering from the Universtity of Twente, Enschede, The Netherlands, in 2001. He joined Ercisson Eurolab, Emmen, The Netherlands, where he worked on CMOS radios for Bluetooth. In 2003, he returned to the IC-Design group of the Universtity of Twente to work towards the Ph.D. degree on the subject of wideband receiver techniques in CMOS. The results of this work are contained in this thesis. In 2008 he joined Axiom IC, Enschede, The Netherlands.

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List of Publications

1. P. van Zeijl, J. W. T. Eikenbroek, P. P. Vervoort, S. Setty, J. Tangenberg, G. Shipton, E. Kooistra, I. C. Keekstra, D. Belot, K. Visser, E. Bosma, and S. C. Blaakmeer, "A Bluetooth radio in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1679-1687, Dec. 2002.

2. S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "A wideband noise-canceling CMOS LNA exploiting a transformer," in *Digest of Papers Radio Frequency Integrated Circuits Symposium*, June 2006, pp. 137-140.

3. S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "A wideband Noise-Canceling CMOS LNA exploiting a transformer," *Proceedings of the 17th ProRISC workshop on Circuits, Systems and Signal Processing*, Nov. 2006.

4. S. C. Blaakmeer, E. A. M. Klumperink, B. Nauta, and D. M. W. Leenaerts, "An inductorless wideband balun-LNA in 65nm CMOS with balanced output," in *Proceedings of the 33rd European Solid-State Circuits Conference*, Sept. 2007, pp. 364-367.

5. S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband CMOS Low Noise Amplifierincluding an Active Balun," *Proceedings of the 18th ProRISC workshop on Circuits, Systems and Signal Processing,* Nov. 2007.

6. S.C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "A Wideband Balun LNA I/Q-Mixer combination in 65nm CMOS," in *ISSCC Digest of Technical Papers*, Feb. 2008, pp. 326-327.

7. S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband Balun-LNA with Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1341-1350, June 2008.

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9. S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "The BLIXER, a Wideband Balun-LNA-I/Q-Mixer Topology," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2706-2715, Dec. 2008.

List of Abbreviations

ADC	Analog to Digital Converter
BALUN	BALanced to UNbalanced converter (or vise-versa)
BLIXER	Balun-LNA-mixer
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
DA	Distributed Amplifier
DSB NF	Double SideBand Noise Figure
FCC	Federal Communications Commission
GPS	Global Positioning System
GSM	Global System for Mobile communications
HR	Harmonic Rejection
IC	Integrated Circuit
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
MBOA	Multiband OFDM Alliance
MPW	Multi Project Wafer
NF	Noise Figure

OFDM	Orthogonal Frequency Division Multiplexing
PCB	Printed Circuit Board
RF	Radio Frequency
Rx	Receiver
SDR	Software Defined Radio
SSB NF	Singe SideBand Noise Figure
Tx	Transmitter
UWB	Ultra WideBand
WLAN	Wireless Local Area Network
QSM	Quadrature Sampling Mixer